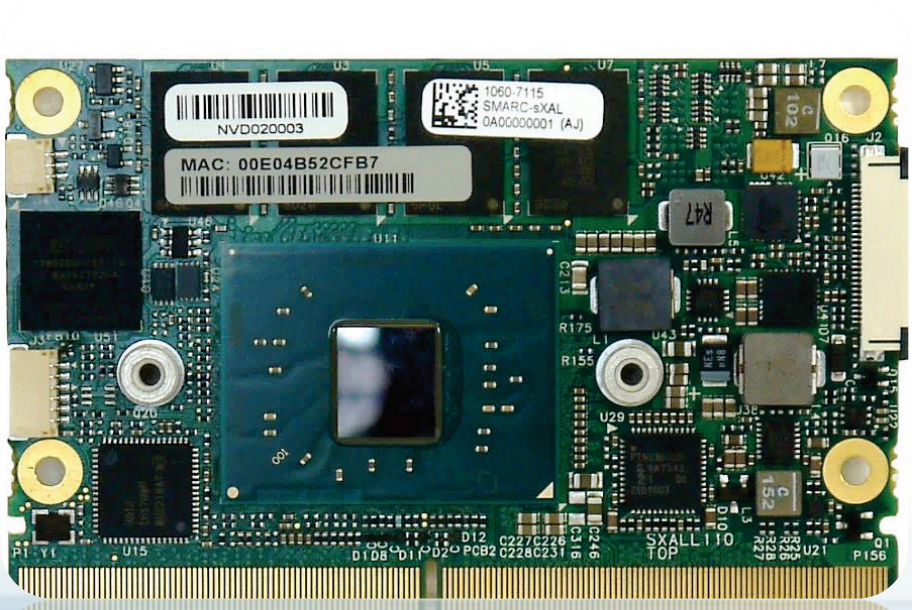
USER GUIDE



SMARC-sXAL

User Guide Rev. 1.95

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SMARC-SXAL – USER GUIDE

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⚠CAUTION

Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Please follow the “General Safety Instructions” supplied with the system.

NOTICE

You find the most recent version of the “General Safety Instructions“ online in the download area of this product.

Revision History

Revision	Brief Description of Changes	Date of Issue	
1.0	initial issue	2017-Jan-20	hjs
1.1	new product numbers	2017-Oct-26	hjs
1.2	added chapter I2C/SMBus	2017-Nov-13	hjs
1.3	added heatspreader documentation	2017-Nov-23	hjs
1.4	added verification data	2017-Nov-27	hjs
1.5	added BIOS chapter	2017-Dec-04	hjs
1.6	wrong BIOS command	2018-Mar-07	hjs
1.7	added information in chapter 5.2	2018-Jul-11	hjs
1.8	added OS versions	2018-Jul-24	hjs
1.9	updated tables in chapter 6.5	2018-Aug-28	hjs
1.91	boot options for the SMARC-sXAL, supported SPI on carrier board	2018-Oct-09	hjs
1.92	Block diagram added	2018-Dec-13	hjs
1.93	MTBF added, design updated, eMMC pSLC info	2019-06-13	hjs
1.94	corrections in Table 1: Component Main Data and Table 1Table 7	2020-07-28	hjs
1.95	Word2016 issues	2021-04-06	hjs

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For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

Symbols

The following symbols may be used in this manual

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or
modifications to the product, that are not explicitly approved by Kontron and described in this User Guide or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version, that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present User Guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.
Kontron follows the WEEE directive
You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Table of Contents

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1/ Introduction

This manual describes the Smart Mobility ARChitecture (SMARC) sXAL board. The use of this Users Guide implies a basic knowledge of PC hard- and software. This manual is focussed on describing the special features and is not intended to be a standard PC textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the CPU board is either done automatically or manually by the user via the BIOS setup menus.

Latest revision of this manual, datasheet, BIOS, drivers and BSP's (Board Support Packages) can be downloaded from Kontron Web Page.

2/ Description

The SMARC-sXAL is a SMARC half-size module using the Intel Apollo Lake-I processor based on Intel x86 SoC. It is designed on the latest SMARC 2.0 specification.

Figure 1: Half-size Card with SMARC interface

Main characteristics are:

- 1x channel LPDDR3L support 8x memory down and 1x ECC, support maximum memory size up to 8 Gbyte
- 4x PCIe x1 Gen 2
- 1x GbE LAN
- 2x USB 3.0/2.0 (SMARC port 2,3)
- 4x USB2.0 Host (SMARC port 0,1,4,5)
- 1x USB2.0 On-the-Go (OTG) (SMARC port 0, via switch of full functional OTG)
- 1x Dual Channel LVDS/1x optional eDP
- 1x HDMI/optional DP
- 1x DP
- Up to 64GB embedded Multimedia Card (eMMC pSLC)
- 1x Secure Digital Input Output (SDIO)
- 1x SPI external Boot (SPI0)
- 1x SPI for generic devices (SPI1)
- 1x HDA Audio
- 1X I2S Audio
- 5x I2C interface
- 1x SMB interface, SMBUS via GPIO controlled switch
- 2x Camera Serial Interface (CSI) of the Mobile Industry Processor Interface (MIPI-CSI2)
- 4x Universal Asynchronous Receiver Transmitter (UART) interfaces
- 12x General-purpose input/output (GPIO)
- Onboard Complex Programmable Logic Device (CPLD)
- SMARC short module form factor (82 mm x 50 mm)

3/ Installation procedure

3.1. Packing Check List

The package includes the following basic items accompany with this manual.

- One board

If this item is damaged or missed, please contact your vendor and save all packing materials for future replacement and maintenance.

Note: The above packing list is for standard single box packing only.

3.2. Requirements IEC62368-1

Take care when designing chassis interface connectors in order to fulfil the IEC62368-1 standard.

Users of board must evaluate the end product to ensure compliance the requirements of the IEC62368-1 safety standard are met:

The motherboard must be installed in a suitable mechanical, electrical and fire enclosure.

The system in its enclosure must be evaluated for temperature and air flow considerations.

For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from or to the product shall be with Safety Extra Low Voltage (SELV) circuits only.

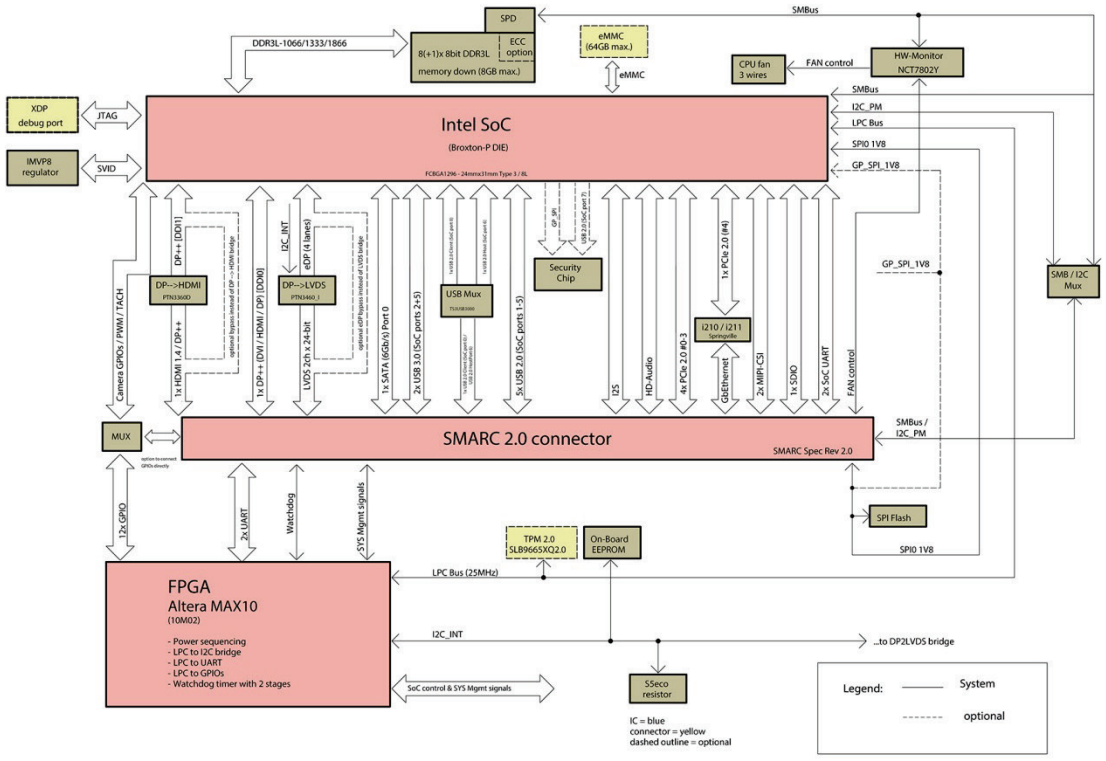
Wires have suitable rating to withstand the maximum available power.

The enclosure of the peripheral device fulfills the fire protecting requirements of IEC62368-1.

4/ System specifications

4.1. Block Diagram

Figure 2: Block Diagram SMARC sXAL



4.2. Component Main Data

The table below summarizes the features of the motherboard.

Table 1: Component Main Data

SMARC-sXAL	
Form factor	Smart Mobility ARChitecture (SMARC) Hardware with 82 mm x 50 mm, max. height 3 mm
Processor	The processor family is Intel Apollo Lake which is a 14 nm / 24 x 31 mm² Type 3; 0.594 mm pitch; 1296 pin count.
BIOS	Onboard 128 Mb SPI flash for BIOS storage
Embedded Controller	FPGA MAX10 for Embedded Feature set and logic control
Memory	1x LPDDR3L 1.35V Memory up to 8 GB, (ECC optional), eight plus one soldered chips
Storage	8 to 64 GB pSLC eMMC 5.0 Flash (option)
Watchdog Timer	Watchdog timer will be supported by WDT Out
Wake On	Wake on LAN
H/W Status Monitor	The SMARC-sXAL design shall incorporate a Nuvoton NCT7802Y hardware monitor. It delivers: ▶ SM Bus connection to the System on Chip (SoC) ▶ Fan control for on-board fan header ▶ PWM and Tach interface to SMARC connector to satisfy SMARC specification ▶ Temperature measurement of the SMARC PCB (2x with external thermal diode) ▶ A/D measurements on V_RTC, V_1V35_S3 and V_3V0-525_IN
Trusted Platform Module (TPM)	incorporated
Complex Programmable Logic Devices (CPLD)	The SMARC-sXAL design shall incorporate a Altera MAX10 CPLD controller which will handle the following. ▶ Power Sequencing ▶ Status and control signal level shifting mostly to allow signals routed to SMARC connector to comply with SMARC Specifications. ▶ Incorporated with a LPC to UART bridge to provide two 2-wire UART. ▶ Incorporated with a LPC to I2C bridge to provide I2C interface. ▶ Incorporated with a LPC to GPIO bridge to provide twelve GPIOs.
Power management	C0, C1, C6, C7, C8, C9, C10
Expansion	The SOC provides four PCIe Gen 2 lanes that can be configured as 4 x 1 (i.e. 4 PCIe links that are x1 wide) or as 1x4 (one link in an x4 configuration). The PCIe links and support signals are to be implemented as per the SMARC specification document.
Operating System Support	Six different Board Support Packages are offered: ▶ BSP1: Windows 10 IOT Enterprise 64 bit, pSLC eMMC Boot ▶ BSP2: Windows 10 IOT Core, Redstone 64 bit ▶ BSP3: Windows 7, 64 bit, pSLC eMMC boot (optional) ▶ BSP4: Windows ES 7, 64 bit, pSLC eMMC boot (optional) ▶ BSP5: Linux 64 bit, Yocto ▶ BSP6: VxWorks 7.x or newer (optional) API: KEAPI 3 for all OS (except for VxWorks)
SMARC I/O System Interconnection	
LAN, USB	1x Gbit-Ethernet, 2x USB3.0 and 4x USB2.0

Audio	1x High Definition Audio (HDA)
Display Port	1x embedded Display Port (eDP) interface. The Intel SoC eDP port shall be used to create the SMARC eDP interface which are sharing the same pins with the LVDS interface.
HDMI	1x HDMI interface. The Intel SoC DDI port shall be used to create the SMARC HDMI interface which are sharing the same pins with the DP++ interface.
LVDS	The Intel SoC eDP shall be used to create the SMARC dual channel LVDS interface. The interface should be able to support 18 and 24 bit single and dual channel LVDS panels.
SMARC I/O System Interconnection	
SATA	1x Gen3 SATA link
GbE LAN	1x SMARC GBE port using Intel I210/I211 PCIe – GBE MAC/PHY controller
LVDS	1x LVDS and one LVDS/eDP
PCIe	4x PCIe Gen 2 lanes that can be configured as 4 x1, i.e. 4 PCIe links that are x1 wide. Or it can be designed as 1x4 with one link in an x4 configuration.
Inter-IC Sound (I2S)	1x I2S interface
Serial Port	2x 2-wire UART interface (TX, RX) and 2x 4-wire UART interface (TX, RX, CTS, RTS) at 1.8 V TTL
Serial Peripheral Interface (SPI)	1x SPI interface which is connected to the primary SPI chip and can also be used for external boot from the BIOS SPI chip.
I2C	5x I2C interfaces which are derived from the SoC
GPIO	12x general purpose inputs/outputs
Internal Header and Jumper	
Sys-Fan	if needed, the fan will operate from the 3 V to 5.25 V input. The fan connector will have on board fan speed control support from the Hardware Monitor chip.
Power	1x 10-pin power connector: The SMARC-sXAL is supplied from a single power supply supporting a voltage of 5 V. Considered current rating of protective device is part of End-Equipment. The SMARC specification defines a maximum current per input voltage pin of 0.5 A. Fan will only operate on 5 V DC.
Display	
Graphics Interface	The board supports onboard graphics through four Ports: ▶ LVDS: The Intel SoC eDP (embedded Display Port) delivers the SMARC dual channel LVDS interface. The interface supports 18 and 24 bit single and dual channel LVDS panels via PTN3460. ▶ eDP: The Intel SoC eDP (embedded Display Port) connect the display via the SMARC eDP interface, which shares the same pins with the LVDS interface. ▶ Dual mode HDMI: Dual Mode (HDMI and DisplayPort on the same pins) implementations are realized through the Intel SoC DDI0 interface. ▶ DP++: The Intel SoC DDI0 shall be used to create the SMARC DP++ interface
Graphics Controller	Intel HD Gfx Gen9
Resolution	DP: 4096 x 2160 @ 60 Hz LVDS: 1920 x 1200 Hz @ 60 Hz eDP: 3840 x 2160 @ 60 Hz HDMI: 3840 x 2160 @ 30 Hz
Ethernet	
Controller	Intel i210IT/i211AT
Interface	one GB Ethernet port via SMARC I/O

Security	
Kontron Security Solution Approtect	The board is equipped with the Kontron Security Solution Approtect, providing an embedded hardware security solution that enables applications to be secured, even in unsecure environments. The solution provides features such as: ▶ Copy protection ▶ IP protection ▶ License model enforcement

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

Table 2: Environmental Conditions

Operating	commercial grade: 0°C to +60°C extended (E1): -25°C to 75°C industrial grade (E2): -40°C to +85°C relative humidity (non-condensing) 10 % to 90 %
Storage	commercial grade: -30°C to +85°C extended (E1): -25°C to 75°C industrial grade (E2): -40°C to +85°C relative humidity (non-condensing) 10 % to 95 %
Electromagnetic Compatibility (EMC) and Interference (EMI)	CE according to (EMC) Directive 2014/30/EU (EN55032, EN55024)
Shock	according to IEC/EN60068-2-6 and IEC/EN60068-2-27
Vibration	According to IEC/EN60068-2-6 and IEC/EN60068-2-27
Electrical Safety	▶ CE according to low Voltage Directive 2014/35/EU (EN62368-1) ▶ Component Recognition to UL62368-1
Theoretical MTBF	680149 hours @ 40°C
Restriction of Hazardous Substances (RoHS) II Compliance	The product will comply to the European Council Directive on the approximation of the laws of the member states relating to Directive 20011/65/EU or the last status thereof. Components and materials of the product must not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE). (Directive 2002/95/EC)
Safety	Component Recognition to UL60950-1

5/ Connectors

5.1. Hardware Configuration Settings

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on the board are in the proper position. The default settings shipped from factory are marked with an asterisk (*).

In general, jumpers on the board are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here, NC stands for “Not Connect”.

5.1.1. Connectors

Table 3: Connectors of SMARC-sXAL

Connector	Function	Remark
SYS_FAN	Sys Fan Connector	1x 3-pin Connector
CPLD	CPLD Connector	1x 6-pin Connector
SMARC	Central Interface	1x 314-pin header

5.1.2. Internal Configuration: I2C and SMBus

Figure 2 shows available I2C buses on the SMARC connector. There is also SMBus available on I2C_PM bus pins. It is selectable with BIOS option.

NOTICE

SMBUS on module is always present, the switch for I2C_PM/SMBUS only controls the I2C or SMBUS interface to the carrier board.

Here is how you can switch between SMBUS and I2C_PM to the carrier board.

1. Hit "DELETE" upon boot up.
2. BIOS menu appears
3. In BIOS Menu, go to the "Advanced" Tab and look for "SMARC Carrier Settings"
4. Choose I2C or SMBus Controller to be routed to carrier board

NOTICE

Check chapter 7/ for more details.

Figure 3: Available I2C buses

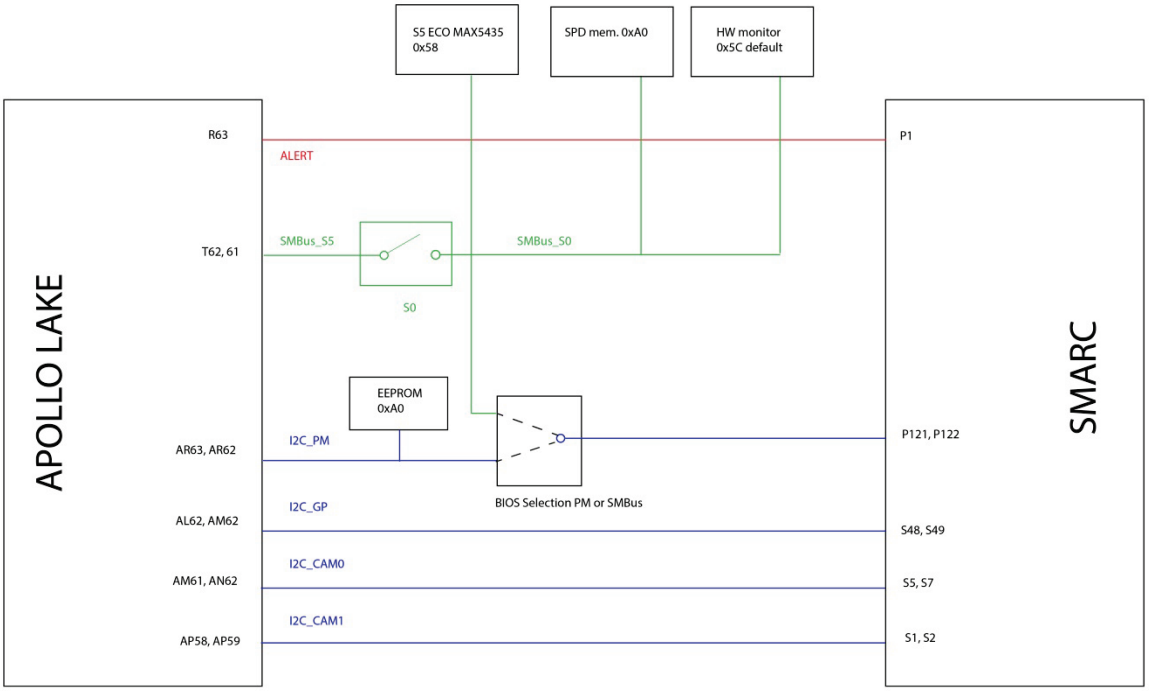


Table 4: I2C_PM devices on SMARC-sXAL

8-bit address	7-bit address	Devices	Notes
0xA0	0x50	EEPROM 24C32 for Board ID	Switched as I2C
0x58	0x2C	MAX5435 S5 eco resistor	Switched as SMBus
0xA0	0x50	DDR3L DRAM0 SPD CAT34C02HU4IGT4A	
0x5C	0x2E	HW monitor NCT7802Y	

Table 5: I2C_INT devices on SMARC-sXAL

8-bit address	7-bit address	Devices	Notes
0xC0	0x60	eDP-->LVDS Bridge PTN3460I	

5.2. Mainboard view and I/O locations

Figure 4: Top View

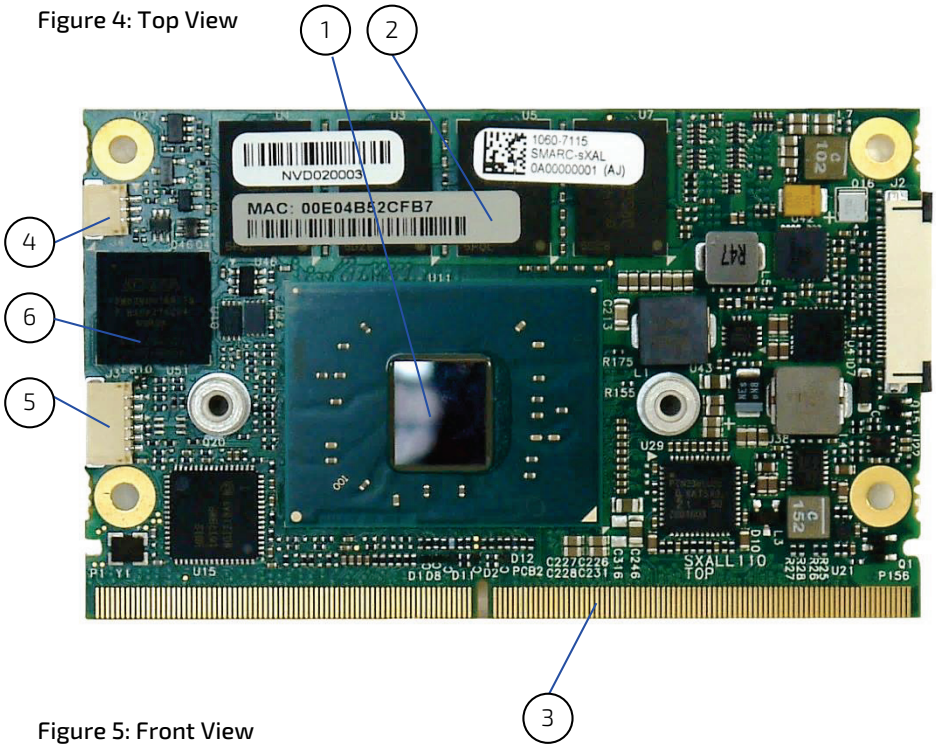
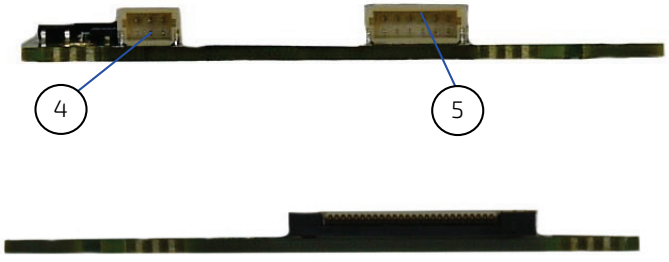


Figure 5: Front View

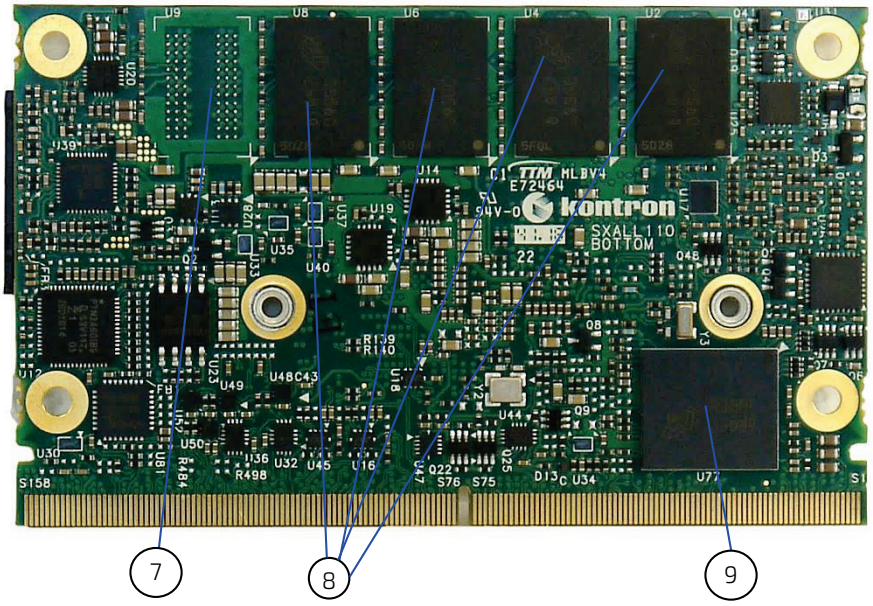
Figure 6: Back View



1. CPU
2. Memory
3. SMARC connector
4. CPU Fan
5. CPLD connector
6. CPLD

5.3. Rear Side

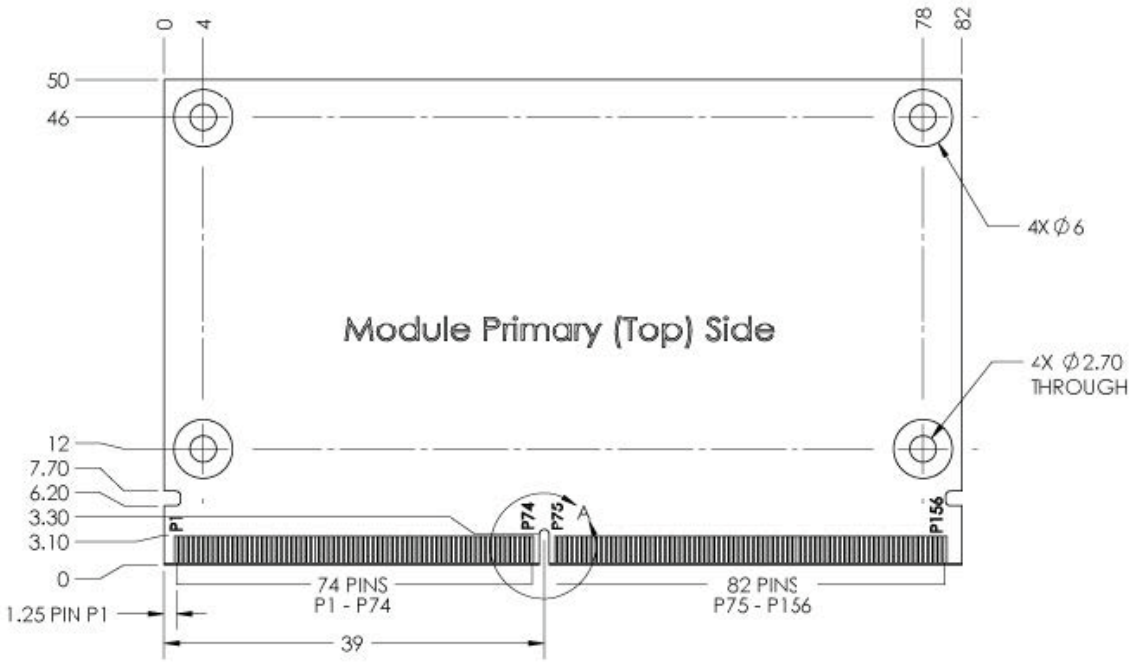
Figure 7: Rear Side from SMARC-sXAL



7. optional ECC-memory location
8. memory
9. pSLC eMMC

5.4. Mechanical Drawing

Figure 8: Mechanical Drawing from SMARC-sXAL



5.5. Thermal Management, Heatspreader and Cooling Solutions

A heatspreader plate assembly is available from Kontron for the SMARC-sXAL. The heatspreader plate on top of this assembly is NOT a heat sink. It works as a SMARC-standard thermal interface to use with a heat sink or external cooling devices.

Figure 9: Heatspreader as cooling solution

External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature on any spot of the heatspreader's surface according the module specifications:

- 60°C for commercial grade modules

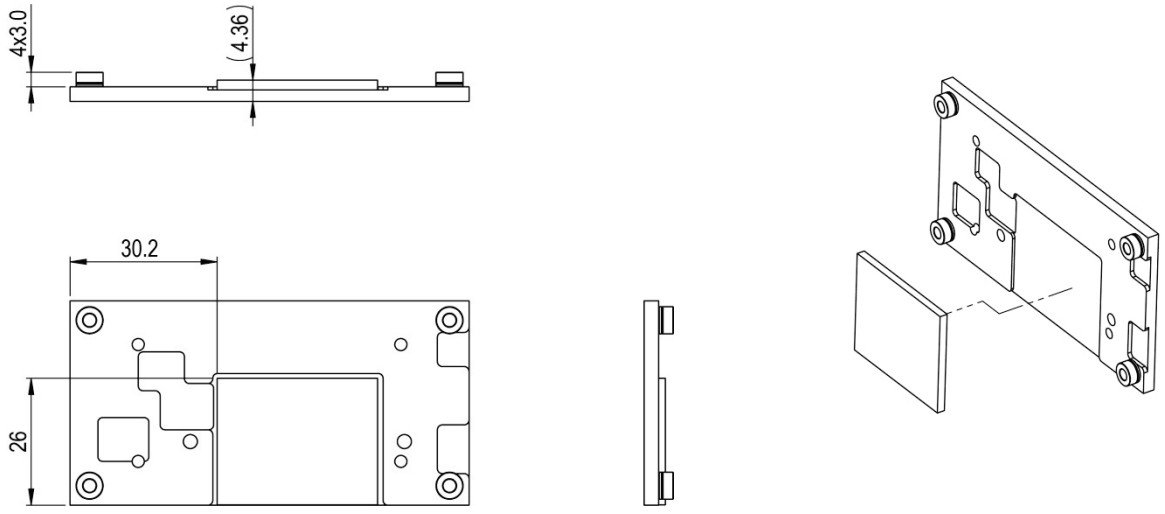
- 75°C for extended temperature grade modules (E1)
- 85°C for industrial temperature grade modules (E2/XT)

The aluminum slugs and thermal pads or the heat-pipe on the underside of the heatspreader assembly implement thermal interfaces between the heatspreader plate and the major heat-generating components. About 80 % of the power dissipated within the module is conducted to the heatspreader plate and can be removed by the cooling solution. Documentation and CAD drawings of heatspreader and cooling solutions are provided at http://emdcustomersection.kontron.com.

5.6. Mechanical Dimensions Heatspreader

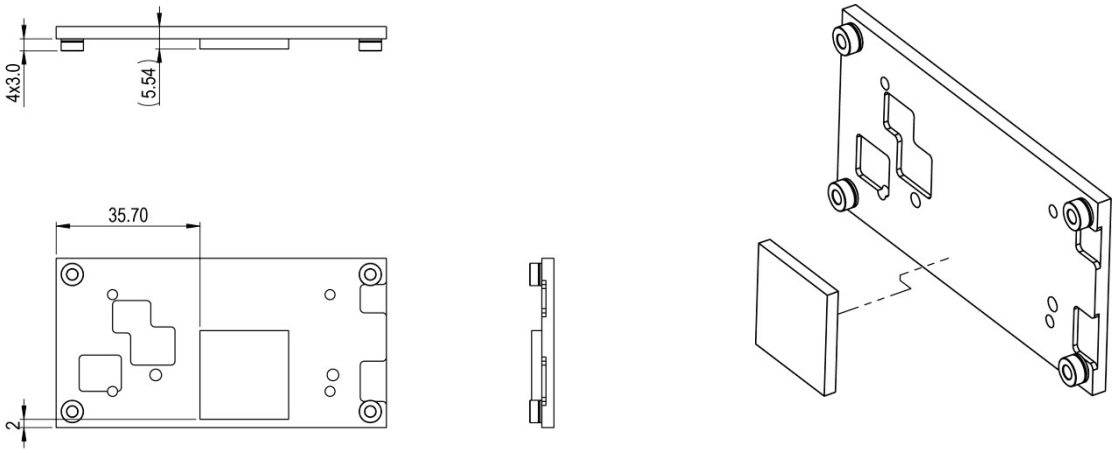
5.6.1. Heatspreader Part-Number 1060-8776 for Industrial Variants

Figure 10: Heatspreader Part-Number 1060-8776



5.6.2. Heatspreader Part-Number 1060-8777 for Commercial Variants

Figure 11: Heatspreader Part-Number 1060-8777



6/ Pin Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.
The connector definitions follow the following notation:

Table 6: Connector Definitions

Column Name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation "XX#" states that the signal "XX" is active low.
Type	AI: Analog Input AO: Analog Output I: Input, TTL compatible if nothing else stated IO: Input / Output, TTL compatible if nothing else stated IOT: Bi-directional tristate IO pin. IS: Schmitt-trigger input, TTL compatible. IOC: Input / open-collector Output, TTL compatible IOD: Input / Output, CMOS level Schmitt-triggered (Open drain output) NC: Not Connected O: Output, TTL compatible OC: Output, open-collector or open-drain, TTL compatible OT: Output with tri-state capability, TTL compatible LVDS: Low Voltage Differential Signal PWR: Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal
Designation	Type and number of item described

6.1. Processor Support

Kontron has defined the board versions as listed in the following table, so far all based on Embedded CPUs.

Industrial Grade:

- Intel Atom x5 E3930 2C 1.8 GHz, 6,5 W (Entry SKU of Apollo Lake @ -40°C to 85°C)
- Intel Atom x5 E3940 4C 1.8 GHz, 9,5 W (Intermediate SKU of Apollo Lake @ -40°C to 85°C)
- Intel Atom x7 E3950 4C 2.0 GHz, 12 W (High SKU of Apollo Lake @ -40°C to 85°C)

Commercial Grade:

- Intel Mobile Celeron N3350 2C 2.3 GHz 6 W (Entry SKU @ 0°C to 60°C)
- Intel Pentium N4200 4C 2.5 GHz 6 W (High SKU @ 0°C to 60°C)

Table 7: Processor Support

Name	Product number	Speed	Embed.	Cache	Sspec	TDP / Tj
Atom x5 E3930 2C	51008-0408-13-5	1.8 GHz	Yes	2 MB	SREKA	6,5 W/85°C
Atom x5 E3940 4C	51008-0832-16-5	1.8 GHz	Yes	2 MB	SREK6	9.5 W/85°C
Atom x7 E3950 4C	51008-0832-16-7	2 GHz	Yes	2 MB	SREK9	12 W/85°C
Mobile Celeron N3350 2C	51007-0408-11-2	2.4 GHz	Yes	2 MB	SREKH	6 W/105°C
Pentium N4200 4C	51007-0832-11-4	2.5 GHz	Yes	2 MB	SRGVZ	6 W/105°C

6.2. System Memory Support

The memory system has one LPDDR3L socket. The sockets support the following memory features:

- 1x Low Power DDR LPDDR3L with 1.35 V
- Max up to 8 GB (8 + 1 chip).
- DDR3-1867 (-1600) memory, ECC for Atom-versions

Kontron offers the following memory modules:

Table 8: Memory Support

Memory Module Description
2 GByte DDR3L
4 GByte DDR3L
8 GByte DDR3L

6.3. Fan Connector

The CPU Fan can be used to power, control and monitor a fan for chassis ventilation etc.

The three-pin header is recommended to be used for driving three-wire type Fan in order to implement Fan speed control.

Figure 12: 3-pin Fan Connector

1

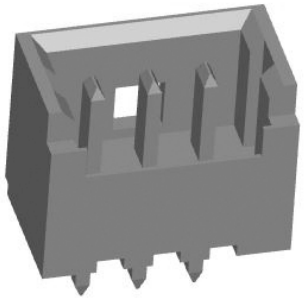


Table 9: 3-pin Fan Connector Pinout

Pin	Signal	Description	Type
1	PWM	Fan speed sense (RPM)	O
2	PWR	Supply for fan	PWR
3	GND	Ground	PWR

6.4. CPLD programming header

Figure 13: 6-pin CPLD Connector

Table 10: 6-pin CPLD Connector

Pin	Signal
1	3.3V Supply
2	TDO
3	TDI
4	TCK
5	TMS
6	GND

6.5. eMMC Flash Memory

An optional embedded Multimedia Flash Card (eMMC) complying with the eMMC 5.0 specification can be permanently attached to the module, allowing for a capacity of up to 64 GByte NAND Flash. During the COMe-cAL6's manufacturing process, Multi Level Cell (MLC) eMMC is reconfigured to act as a pseudo Single Level Cell (pSLC) eMMC to provide improved reliability, endurance and performance.

Specific eMMC Flash memory features are:

- Up to 64 GByte pSLC (or128 GB MLC)
- eMMC 5.0 specification
- Class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
- HS200/HS400 modes
- DDR modes up to 52 MHz clock speed
- ECC and block management
- Boot operation (High-speed boot)
- Sleep mode
- Permanent and power-on write protection
- Replay-protected memory block (RPMB)
- Secure erase and secure trim

6.6. SMARC Connector

The SMARC connector has different pins on both sides:

- Top side: 74 pins are on the left side, 82 pins on the right side
- Bottom side: 75 pins are on the left side, 83 pins on the right side

Figure 14: 314-pin SMARC Connector

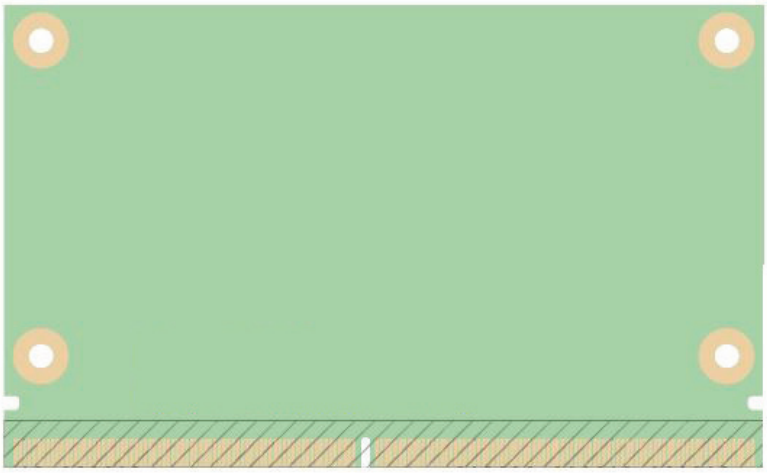


Table 11: P-Pins SMARC Connector

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
P1	SMB_ALERT _1V8#	SM Bus Alert# (interrupt) signal	I-1,8		
P2	GND	Power Ground	PWRGND		
P3	CSI1_CK+	CSI differential clock inputs	DP-I		
P4	CSI1_CK-	CSI differential clock inputs	DP-I		
P5	GBE1_SDP	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol). This is typically implemented by the software-defined pins from the Ethernet controller. The SDP pins can be used for IEEE1588 auxiliary device connections and for other miscellaneous hardware or software-control purposes.	NC		
P6	GBE0_SDP	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol).This is typically implemented by the software-defined pins from the Ethernet controller. The SDP pins can be used for IEEE1588 auxiliary device connections and for other miscellaneous hardware or software-control purposes.	I/O-3,3		
P7	CSI1_RX0+	Differential data pairs used for camera configurations	DP-I		
P8	CSI1_RX0-	Differential data pairs used for camera configurations	DP-I		
P9	GND	Power Ground	PWRGND		
P10	CSI1_RX1+	Differential data pairs used for camera configurations	DP-I		
P11	CSI1_RX1-	Differential data pairs used for camera configurations	DP-I		

Pin	Primary (Top) Side	Description	Type	Termination	Comment
P12	GND	Power Ground	PWRGND		
P13	CSI1_RX2+	Differential data pairs used for camera configurations	DP-I		
P14	CSI1_RX2-	Differential data pairs used for camera configurations	DP-I		
P15	GND	Power Ground	PWRGND		
P16	CSI1_RX3+	Differential data pairs used for camera configurations	DP-I		
P17	CSI1_RX3-	Differential data pairs used for camera configurations	DP-I		
P18	GND	Power Ground	PWRGND		
P19	GBE0_MDI3-	Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface)	DP-I/O		
P20	GBE0_MDI3+	Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface)	DP-I/O		
P21	GBE0_LINK100#	Link Speed Indication LED for 100Mbps. Shall be able to sink 24mA or more Carrier LED current.	OD		3.3V Tolerance
P22	GBE0_LINK1000#	Link Speed Indication LED for 1000Mbps. Shall be able to sink 24mA or more Carrier LED current.	OD		3.3V Tolerance
P23	GBE0_MDI2-	Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface)	DP-I/O		
P24	GBE0_MDI2+	Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface)	DP-I/O		
P25	GBE0_LINK_ACT#	Link / Activity Indication LED: Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity. Shall be able to sink 24mA or more Carrier LED current	OD		3.3V Tolerance
P26	GBE0_MDI1-	Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface)	DP-I/O		
P27	GBE0_MDI1+	Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface)	DP-I/O		
P28	GBE0_CTREF	Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)	NC		
P29	GBE0_MDI0-	Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface)	DP-I/O		
P30	GBE0_MDI0+	Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface)	DP-I/O		
P31	SPI0_CS1#	SPI0 Master Chip Select 1 output	O-1,8		
P32	GND	Power Ground	PWRGND		
P33	SDIO_WP	Write Protect	I-3,3		
P34	SDIO_CMD	Command line	I/O-3,3		
P35	SDIO_CD#	Card Detect	I-3,3		
P36	SDIO_CK	Clock	I/O-3,3		
P37	SDIO_PWR_EN	SD card power enable	O-3,3		
P38	GND	Power Ground	PWRGND		
P39	SDIO_D0	Data path	I/O-3,3		
P40	SDIO_D1	Data path	I/O-3,3		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
P41	SDIO_D2	Data path	I/O-3,3		
P42	SDIO_D3	Data path	I/O-3,3		
P43	SPI0_CS0#	SPI0 Master Chip Select 0 output Use to select Carrier SPI boot device	O-1,8		
P44	SPI0_CK	SPI0 Master Clock output	O-1,8		
P45	SPI0_DIN	SPI0 Master Data input (input to CPU, output from SPI device)	I-1,8		
P46	SPI0_DO	SPI0 Master Data output (output from CPU, input to SPI device)	O-1,8		
P47	GND	Power Ground	PWRGND		
P48	SATA_TX+	Differential SATA 0 transmit data Pair: 0402 series coupling caps shall be on Module	DP-O		
P49	SATA_TX-	Differential SATA 0 transmit data Pair: 0402 series coupling caps shall be on Module	DP-O		
P50	GND	Power Ground	PWRGND		
P51	SATA_RX+	Differential SATA 0 transmit data Pair: 0402 series coupling caps shall be on Module	DP-I		
P52	SATA_RX-	Differential SATA 0 transmit data Pair: 0402 series coupling caps shall be on Module	DP-I		
P53	GND	Power Ground	PWRGND		
P54	ESPI_CS0#	ESPI Master Chip Select Outputs: Driving Chip Select# low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select# pin.	O-1,8		
P55	ESPI_CS1#	ESPI Master Chip Select Outputs: Driving Chip Select# low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select# pin.	O-1,8		
P56	ESPI_CK	ESPI Master Clock Output: This Pin provides the reference timing for all the serial input and output operations	O-1,8		
P57	ESPI_IO_0	ESPI Master Data Input / Outputs: Operate in Single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO).	I-1,8		
P58	ESPI_IO_1	ESPI Master Data Input / Outputs: Operate in Single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO).	O-1,8		
P59	GND	Power Ground	PWRGND		
P60	USB0+	Differential USB 2.0 data pairs	DP-I/O		
P61	USB0-	Differential USB 2.0 data pairs	DP-I/O		
P62	USB0_EN_OC#	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up shall be present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further	Bi-Dir / OD		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
		details may be found in Section 4.10.3 USB[0:5]_EN_OC# Discussion below.			
P63	USB0_VBUS_DET	USB host power detection, when this port is used as a device.	I-5,0		
P64	USB0_OTG_ID	USB OTG ID input, active high.	I-3,3		
P65	USB1+	Differential USB 2.0 data pairs	DP-I/O		
P66	USB1-	Differential USB 2.0 data pairs	DP-I/O		
P67	USB1_EN_OC#	Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up shall be present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 USB[0:5]_EN_OC# Discussion below.	Bi-Dir / OD		
P68	GND	Power Ground	PWRGND		
P69	USB2+	Differential USB 2.0 data pairs	DP-I/O		
P70	USB2-	Differential USB 2.0 data pairs	DP-I/O		
P71	USB2_EN_OC#	Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up shall be present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 USB[0:5]_EN_OC# Discussion below.	Bi-Dir / OD		
P72	RSVD	Reserved	NC		
P73	RSVD	Reserved	NC		
P74	USB3_EN_OC#	Pulled low by Module OD driver to disable USB3 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up shall be present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 USB[0:5]_EN_OC# Discussion below.	Bi-Dir / OD		
P75	PCIE_A_RST#	PCIe Port reset output	O-3,3		
P76	USB4_EN_OC#	Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up shall be present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 USB[0:5]_EN_OC# Discussion below.	Bi-Dir / OD		
P77	RSVD	Reserved	NC		
P78	RSVD	Reserved	NC		
P79	GND	Power Ground	PWRGND		
P80	PCIE_C_REFCK+	Differential PCIe Link reference clock output DC coupled	DP-O		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
P81	PCIE_C_REFCK-	Differential PCIe Link reference clock output DC coupled	DP-O		
P82	GND	Power Ground	PWRGND		
P83	PCIE_A_REFCK+	Differential PCIe Link reference clock output DC coupled	DP-O		
P84	PCIE_A_REFCK-	Differential PCIe Link reference clock output DC coupled	DP-O		
P85	GND	Power Ground	PWRGND		
P86	PCIE_A_RX+	Differential PCIe Link receive data pair 0 No coupling caps on Module	DP-I		
P87	PCIE_A_RX-	Differential PCIe Link receive data pair 0 No coupling caps on Module	DP-I		
P88	GND	Power Ground	PWRGND		
P89	PCIE_A_TX+	Differential PCIe Link transmit data pair Series coupling caps shall be on the Module Caps should be 0402 package 0.1uF	DP-O		
P90	PCIE_A_TX-	Differential PCIe Link transmit data pair Series coupling caps shall be on the Module Caps should be 0402 package 0.1uF	DP-O		
P91	GND	Power Ground	PWRGND		
P92	HDMI_D2+ / DP1_LANE0+	TMDS / HDMI data differential pairs or DP1 lane pairs	DP-O		
P93	HDMI_D2- / DP1_LANE0-	TMDS / HDMI data differential pairs or DP1 lane pairs	DP-O		
P94	GND	Power Ground	PWRGND		
P95	HDMI_D1+ / DP1_LANE1+	TMDS / HDMI data differential pairs or DP1 lane pairs	DP-O		
P96	HDMI_D1- / DP1_LANE1-	TMDS / HDMI data differential pairs or DP1 lane pairs	DP-O		
P97	GND	Power Ground	PWRGND		
P98	HDMI_D0+ / DP1_LANE2+	TMDS / HDMI data differential pairs or DP1 lane pairs	DP-O		
P99	HDMI_D0- / DP1_LANE2-	TMDS / HDMI data differential pairs or DP1 lane pairs	DP-O		
P100	GND	Power Ground	PWRGND		
P101	HDMI_CK+ / DP1_LANE3+	HDMI differential clock output pair or DP1 lane pairs	DP-O		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
P102	HDMI_CK- / DP1_LANE3-	HDMI differential clock output pair or DP1 lane pairs	DP-O		
P103	GND	Power Ground	PWRGND		
P104	HDMI_HPD / DP1_HPD	HDMI/DP1 Hot Plug Detect input	I-1,8		
P105	HDMI_CTRL_CK / DP1_AUX+	I2C clock line dedicated to HDMI or DP1 Auxiliary Channel	O-1,8		
P106	HDMI_CTRL_DAT / DP1_AUX-	I2C data line dedicated to HDMI or DP1 Auxiliary Channel	I/O-1,8		
P107	DP1_AUX_SEL	Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations. Driven to 1.8V on Carrier for HDMI operation. Terminated on Module through 1M resistor to GND.	I-1,8		
P108	GPIO0 / CAM0_PWR#	GPIO or Camera 0 Power Enable, active low output	I/O-1,8		
P109	GPIO1 / CAM1_PWR#	GPIO or Camera 1 Power Enable, active low output	I/O-1,8		
P110	GPIO2 / CAM0_RST#	GPIO or Camera 0 Reset, active low output	I/O-1,8		
P111	GPIO3 / CAM1_RST#	GPIO or Camera 1 Reset, active low output	I/O-1,8		
P112	GPIO4 / HDA_RST#	GPIO or HD Audio Reset, active low output	I/O-1,8		
P113	GPIO5 / PWM_OUT	GPIO or PWM output	I/O-1,8		
P114	GPIO6 / TACHIN	GPIO or Tachometer input (used with the GPIO5 PWM)	I/O-1,8		
P115	GPIO7	General purpose input / output	I/O-1,8		
P116	GPIO8	General purpose input / output	I/O-1,8		
P117	GPIO9	General purpose input / output	I/O-1,8		
P118	GPIO10	General purpose input / output	I/O-1,8		
P119	GPIO11	General purpose input / output	I/O-1,8		
P120	GND	Power Ground	PWRGND		
P121	I2C_PM_CK	Power management I2C bus clock.	I/O-1,8		
P122	I2C_PM_DAT	Power management I2C bus data.	I/O-1,8		
P123	BOOT_SEL0#	Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
P124	BOOT_SEL1#	Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
P125	BOOT_SEL2#	Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
P126	RESET_OUT#	General purpose reset output to Carrier board.	O-1,8		
P127	RESET_IN#	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
P128	POWER_BTN#	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
P129	SER0_TX	Asynchronous serial port data out	O-1,8		
P130	SER0_RX	Asynchronous serial port data in	I-1,8		
P131	SER0_RTS#	Request to Send handshake line for SER0	O-1,8		
P132	SER0_CTS#	Clear to Send handshake line for SER0	I-1,8		
P133	GND	Power Ground	PWRGND		
P134	SER1_TX	Asynchronous serial port data out	O-1,8		
P135	SER1_RX	Asynchronous serial port data in	I-1,8		
P136	SER2_TX	Asynchronous serial port data out	O-1,8		
P137	SER2_RX	Asynchronous serial port data in	I-1,8		
P138	SER2_RTS#	Request to Send handshake line for SER2	O-1,8		
P139	SER2_CTS#	Clear to Send handshake line for SER2	I-1,8		
P140	SER3_TX	Asynchronous serial port data out	O-1,8		
P141	SER3_RX	Asynchronous serial port data in	I-1,8		
P142	GND	Power Ground	PWRGND		
P143	CAN0_TX	CAN Transmit output	NC		
P144	CAN0_RX	CAN Receive input	NC		
P145	CAN1_TX	CAN Transmit output	NC		
P146	CAN1_RX	CAN Receive input	NC		
P147	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		
P148	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		
P149	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		
P150	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		
P151	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		
P152	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		
P153	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		
P154	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		
P155	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		
P156	VDD_IN	Module power input voltage - 3.0V min to 5.25V max	PWR		

Table 12: S-Pins SMARC Connector

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
S1	I2C_CAM1_CK	I2C Camera clock signal	I/O-1,8		
S2	I2C_CAM1_DAT	I2C Camera data signal	I/O-1,8		
S3	GND	Power Ground	PWRGND		
S4	RSVD	Reserved	NC		
S5	I2C_CAM0_CK	I2C Camera clock signal	I/O-1,8		
S6	CAM_MCK	Master clock output for CSI camera support (may be used for CSI0 and / or CSI1)	O-1,8		
S7	I2C_CAM0_DAT	I2C Camera data signal	I/O-1,8		
S8	CSI0_CK+	CSI differential clock inputs	DP-I		
S9	CSI0_CK-	CSI differential clock inputs	DP-I		
S10	GND	Power Ground	PWRGND		
S11	CSI0_RX0+	Differential data pairs used for camera configurations	DP-I		
S12	CSI0_RX0-	Differential data pairs used for camera configurations	DP-I		
S13	GND	Power Ground	PWRGND		
S14	CSI0_RX1+	Differential data pairs used for camera configurations	DP-I		
S15	CSI0_RX1-	Differential data pairs used for camera configurations	DP-I		
S16	GND	Power Ground	PWRGND		
S17	GBE1_MDI0+	Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface)	NC		
S18	GBE1_MDI0-	Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface)	NC		
S19	GBE1_LINK100#	Link Speed Indication LED for 100Mbps: Shall be able to sink 24mA or more Carrier LED current	NC		
S20	GBE1_MDI1+	Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface)	NC		
S21	GBE1_MDI1-	Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface)	NC		
S22	GBE1_LINK1000#	Link Speed Indication LED for 1000Mbps: Shall be able to sink 24mA or more Carrier LED current	NC		
S23	GBE1_MDI2+	Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface)	NC		
S24	GBE1_MDI2-	Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface)	NC		
S25	GND	Power Ground	PWRGND		
S26	GBE1_MDI3+	Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface)	NC		
S27	GBE1_MDI3-	Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface)	NC		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
S28	GBE1_CTREF	Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)	NC		
S29	PCIE_D_TX+	Differential PCIe Link transmit data pair Series coupling caps shall be on the Module Caps should be 0402 package 0.1uF	DP-O		
S30	PCIE_D_TX-	Differential PCIe Link transmit data pair Series coupling caps shall be on the Module Caps should be 0402 package 0.1uF	DP-O		
S31	GBE1_LINK_ACT#	Link / Activity Indication LED: Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity. Shall be able to sink 24mA or more Carrier LED current	NC		
S32	PCIE_D_RX+	Differential PCIe Link receive data pair 3 No coupling caps on Module	DP-I		
S33	PCIE_D_RX-	Differential PCIe Link receive data pair 3 No coupling caps on Module	DP-I		
S34	GND	Power Ground	PWRGND		
S35	USB4+	Differential USB 2.0 data pairs	DP-I/O		
S36	USB4-	Differential USB 2.0 data pairs	DP-I/O		
S37	USB3_VBUS_DET	USB host power detection, when this port is used as a device.	NC		
S38	AUDIO_MCK	Master clock output to Audio codecs	O-1,8		
S39	I2S0_LRCK	Left& Right audio synchronization clock	I/O-1,8		
S40	I2S0_SDOUT	Digital audio Output	O-1,8		
S41	I2S0_SDIN	Digital audio Input	I-1,8V		
S42	I2S0_CK	Digital audio clock	I/O-1,8		
S43	ESPI_ALERT0#	This pin is used by eSPI slave to request service from eSPI master. Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.	NC		
S44	ESPI_ALERT1#	This pin is used by eSPI slave to request service from eSPI master. Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.	NC		
S45	RSVD	Reserved	NC		
S46	RSVD	Reserved	NC		
S47	GND	Power Ground	PWRGND		
S48	I2C_GP_CK	I2C General Purpose clock signal	I/O-1,8		
S49	I2C_GP_DAT	I2C General Purpose data signal	I/O-1,8		
S50	HDA_SYNC	HDA sync Alternative use: I2S2_LRCK	I/O-1,8		
S51	HDA_SDO	High Definition Audio data out Alternative use: I2S2_SDOUT	O-1,8		
S52	HDA_SDI	High Definition Audio data in Alternative use: I2S2_SDI	I-1,8V		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
S53	HDA_CK	High Definition Audio clock Alternative use: I2S2_CK	I/O-1,8V		
S54	SATA_ACT#	Active low SATA activity indicator: If implemented, shall be able to sink 24mA or more Carrier LED current	OD		3.3V Tole-rance
S55	USB5_EN_OC#	Pulled low by Module OD driver to disable USB5 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up shall be present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 USB[0:5]_EN_OC# Discussion below.	Bi-Dir / OD		
S56	ESPI_IO_2	ESPI Master Data Input / Outputs: These are bi-directional input/output pins used to transfer data between master and slaves. In Single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO).	NC		
S57	ESPI_IO_3	ESPI Master Data Input / Outputs: These are bi-directional input/output pins used to transfer data between master and slaves. In Single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO).	NC		
S58	ESPI_RESET#	ESPI Reset: Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves.	NC		
S59	USB5+	Differential USB 2.0 data pairs	DP-I/O		
S60	USB5-	Differential USB 2.0 data pairs	DP-I/O		
S61	GND	Power Ground	PWRGND		
S62	USB3_SSTX+	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	DP-O		
S63	USB3_SSTX-	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	DP-O		
S64	GND	Power Ground	PWRGND		
S65	USB3_SSRX+	Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	DP-I		
S66	USB3_SSRX-	Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	DP-I		
S67	GND	Power Ground	PWRGND		
S68	USB3+	Differential USB 2.0 data pairs	DP-I/O		
S69	USB3-	Differential USB 2.0 data pairs	DP-I/O		
S70	GND	Power Ground	PWRGND		
S71	USB2_SSTX+	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	DP-O		
S72	USB2_SSTX-	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	DP-O		
S73	GND	Power Ground	PWRGND		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
S74	USB2_SSRX+	Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	DP-I		
S75	USB2_SSRX-	Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	DP-I		
S76	PCIE_B_RST#	PCIe Port reset output	O-3,3		
S77	PCIE_C_RST#	PCIe Port reset output	O-3,3		
S78	PCIE_C_RX+	Differential PCIe Link receive data pair 2 No coupling caps on Module	DP-I		
S79	PCIE_C_RX-	Differential PCIe Link receive data pair 2 No coupling caps on Module	DP-I		
S80	GND	Power Ground	PWRGND		
S81	PCIE_C_TX+	Differential PCIe Link transmit data pair Series coupling caps shall be on the Module Caps should be 0402 package 0.1uF	DP-O		
S82	PCIE_C_TX-	Differential PCIe Link transmit data pair Series coupling caps shall be on the Module Caps should be 0402 package 0.1uF	DP-O		
S83	GND	Power Ground	PWRGND		
S84	PCIE_B_REFCK+	Differential PCIe Link reference clock output DC coupled	DP-O		
S85	PCIE_B_REFCK-	Differential PCIe Link reference clock output DC coupled	DP-O		
S86	GND	Power Ground	PWRGND		
S87	PCIE_B_RX+	Differential PCIe Link receive data pair 1 No coupling caps on Module	DP-I		
S88	PCIE_B_RX-	Differential PCIe Link receive data pair 1 No coupling caps on Module	DP-I		
S89	GND	Power Ground	PWRGND		
S90	PCIE_B_TX+	Differential PCIe Link transmit data pair Series coupling caps shall be on the Module Caps should be 0402 package 0.1uF	DP-O		
S91	PCIE_B_TX-	Differential PCIe Link transmit data pair Series coupling caps shall be on the Module Caps should be 0402 package 0.1uF	DP-O		
S92	GND	Power Ground	PWRGND		
S93	DP0_LANE0+	DP Data Pair 0	DP-O		
S94	DP0_LANE0-	DP Data Pair 0	DP-O		
S95	DP0_AUX_SEL	Pulled to GND on Carrier for DP operation in Dual Mode implementations.	I-1,8		
S96	DP0_LANE1+	DP Data Pair 1	DP-O		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
S97	DP0_LANE1 -	DP Data Pair 1	DP-O		
S98	DP0_HPD	Hot plug detection signal.	I-1,8		
S99	DP0_LANE2 +	DP Data Pair 2	DP-O		
S100	DP0_LANE2 -	DP Data Pair 2	DP-O		
S101	GND	Power Ground	PWRGND		
S102	DP0_LANE3 +	DP Data Pair 3	DP-O		
S103	DP0_LANE3 -	DP Data Pair 3	DP-O		
S104	USB3_OTG_ ID	USB OTG ID input, active high.	NC		
S105	DP0_AUX+	Auxiliary channel used for link management and device control. Differential pair lines.	DP-I/O		
S106	DP0_AUX-	Auxiliary channel used for link management and device control. Differential pair lines.	DP-I/O		
S107	LCD1_BKLT _EN	High enables panel backlight	O-1,8		
S108	LVDS1_CK+	LVDS LCD differential clock pair	DP-O		
S109	LVDS1_CK-	LVDS LCD differential clock pair	DP-O		
S110	GND	Power Ground	PWRGND		
S111	LVDS1_0+	LVDS LCD data channel differential pairs	DP-O		
S112	LVDS1_0-	LVDS LCD data channel differential pairs	DP-O		
S113	eDP1_HPD	eDP1 Hot Plug Detect pins	I-1,8		
S114	LVDS1_1+	LVDS LCD data channel differential pairs	DP-O		
S115	LVDS1_1-	LVDS LCD data channel differential pairs	DP-O		
S116	LCD1_VDD_ EN	High enables panel VDD	O-1,8		
S117	LVDS1_2+	LVDS LCD data channel differential pairs	DP-O		
S118	LVDS1_2-	LVDS LCD data channel differential pairs	DP-O		
S119	GND	Power Ground	PWRGND		
S120	LVDS1_3+	LVDS LCD data channel differential pairs	DP-O		
S121	LVDS1_3-	LVDS LCD data channel differential pairs	DP-O		
S122	LCD1_BKLT _PWM	Display backlight PWM control	O-1,8		
S123	RSVD	Reserved	NC		
S124	GND	Power Ground	PWRGND		
S125	LVDS0_0+ / eDP0_TX0+	LVDS LCD data channel differential pairs, eDP data pairs	DP-O		
S126	LVDS0_0- / eDP0_TX0-	LVDS LCD data channel differential pairs, eDP data pairs,	DP-O		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
S127	LCD0_BKLT_EN	High enables panel backlight	O-1,8		
S128	LVDS0_1+ / eDP0_TX1+	LVDS LCD data channel differential pairs, eDP data pairs,	DP-O		
S129	LVDS0_1- / eDP0_TX1-	LVDS LCD data channel differential pairs, eDP data pairs,	DP-O		
S130	GND	Power Ground	PWRGND		
S131	LVDS0_2+ / eDP0_TX2+	LVDS LCD data channel differential pairs, eDP data pairs,	DP-O		
S132	LVDS0_2- / eDP0_TX2-	LVDS LCD data channel differential pairs, eDP data pairs,	DP-O		
S133	LCD0_VDD_EN	High enables panel VDD	O-1,8		
S134	LVDS0_CK+ / eDP0_AUX+	LVDS LCD differential clock pair, eDP Auxiliary channel,	DP-O / DP-I/O		
S135	LVDS0_CK- / eDP0_AUX-	LVDS LCD differential clock pair, eDP Auxiliary channel,	DP-O / DP-I/O		
S136	GND	Power Ground	PWRGND		
S137	LVDS0_3+ / eDP0_TX3+	LVDS LCD data channel differential pairs, eDP data pairs	DP-O		
S138	LVDS0_3- / eDP0_TX3-	LVDS LCD data channel differential pairs, eDP data pairs	DP-O		
S139	I2C_LCD_CK	I2C clock – to read LCD display EDID EEPROMs	I/O-1,8		
S140	I2C_LCD_DAT	I2C data – to read LCD display EDID EEPROMs Be aware of possible EDID PROM address conflicts if multiple displays are implemented	I/O-1,8		
S141	LCD0_BKLT_PWM	Display backlight PWM control	O-1,8		
S142	RSVD	Reserved	NC		
S143	GND	Power Ground	PWRGND		
S144	eDP0_HPD	eDP0 Hot Plug Detect pins	I-1,8		
S145	WDT_TIME_OUT#	Watch-Dog-Timer Output	O-1,8		
S146	PCIE_WAKE#	PCIe wake up interrupt to host – common to PCIe links A, B, C, D – pulled up or terminated on Module	I-3,3		
S147	VDD_RTC	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.	Power In Power Out (when charging a Super Cap)		
S148	LID#	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low,	I-1,8		

Pin	Primary (Top) Side	Description	Type	Termi-nation	Comment
		level sensitive. Should be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.			
S149	SLEEP#	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
S150	VIN_PWR_BAD#	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
S151	CHARGING#	Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
S152	CHARGER_PRSNT#	Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
S153	CARRIER_STBY#	The Module shall drive this signal low when the system is in a standby power state. On x86 designs this pin should utilize the SUS_S3# signal.	O-1,8		
S154	CARRIER_PWR_ON	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal. On x86 designs this pin should utilize the SUS_S5# signal, but then it shall maintain still the CARRIER_PWR_ON functionality to avoid back driving.	O-1,8		
S155	FORCE_RECOV#	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults.	I-1,8		
S156	BATLOW#	Battery low indication to Module. Carrier to float the line in in-active state. Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
S157	TEST#	Held low by Carrier to invoke Module vendor specific test function(s). Pulled up on Module. Driven by OD part on Carrier.	I-1,8		
S158	GND	Pulled up on Module. Driven by OD part on Carrier.	PWRGND		

Table 13: Legend

Signal	Description
I-1,8	1.8 V Input

Signal	Description
DP-I	Differential Pair Input
DP-I/O	Differential Pair Input/Output
I/O-3,3	Bi-directional 3.3 V I/O signal
I-3,3	3.3 V Input
PWRGND	Power Ground
OD	Output Open Drain
NC	Not Connected (on this product)
O-1,8	1.8 V Output
DP-O	Differential Pair Output
I/O-1,8	Bi-directional 1.8 V I/O signal
I-5,0	5.0 V Input
O-3,3	3.3 V Output

7/ uEFI BIOS

7.1. Starting the uEFI BIOS

The board is provided with a Kontron-customized, pre-installed and configured version of American Megatrends, Inc. (AMI). It is based on the Unified Extensible Firmware Interface (uEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features.

The BIOS version covered in this document might not be the latest version. The latest version might have certain differences to the BIOS options and features described in this chapter.

The uEFI BIOS comes with a Setup program which provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The Setup program allows the accessing of various menus which provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS Setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A Setup menu will appear.

The uEFI BIOS Setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the Setup screens.

The following table provides information concerning the usage of these hot keys.

Table 14: Navigation Hot Keys Available in the Legend Bar

Hotkeys	Description
<F1>	The <F1> key is used to invoke the General Help window.
<->	The<Minus> key is used to select the next lower value within a field.
<+>	The <Plus> key is used to select the next higher value within a field.
<F4>	The <F4> key is used to Exit saving Changes.
<F3>	The <F3> key is used to load Optimized Defaults.
<→> or <←>	The <Left/Right> arrows are used to select major Setup menus on the menu bar. For example: Main screen, Advanced screen, Security screen, etc.
<↑> or <↓>	The <Up/Down> arrows are used to select fields in the current menu. For example a Setup function or a sub-screen.
<ESC>	The <ESC> key is used to exit a Setup menu.
<RETURN>	The <RETURN> key is used to execute a command or select a submenu.

7.2. Setup Menus

The Setup utility features a selection bar at the top of the screen that lists the available menus:

1. Main
2. Advanced
3. Chipset
4. Security
5. Boot
6. Save & Exit

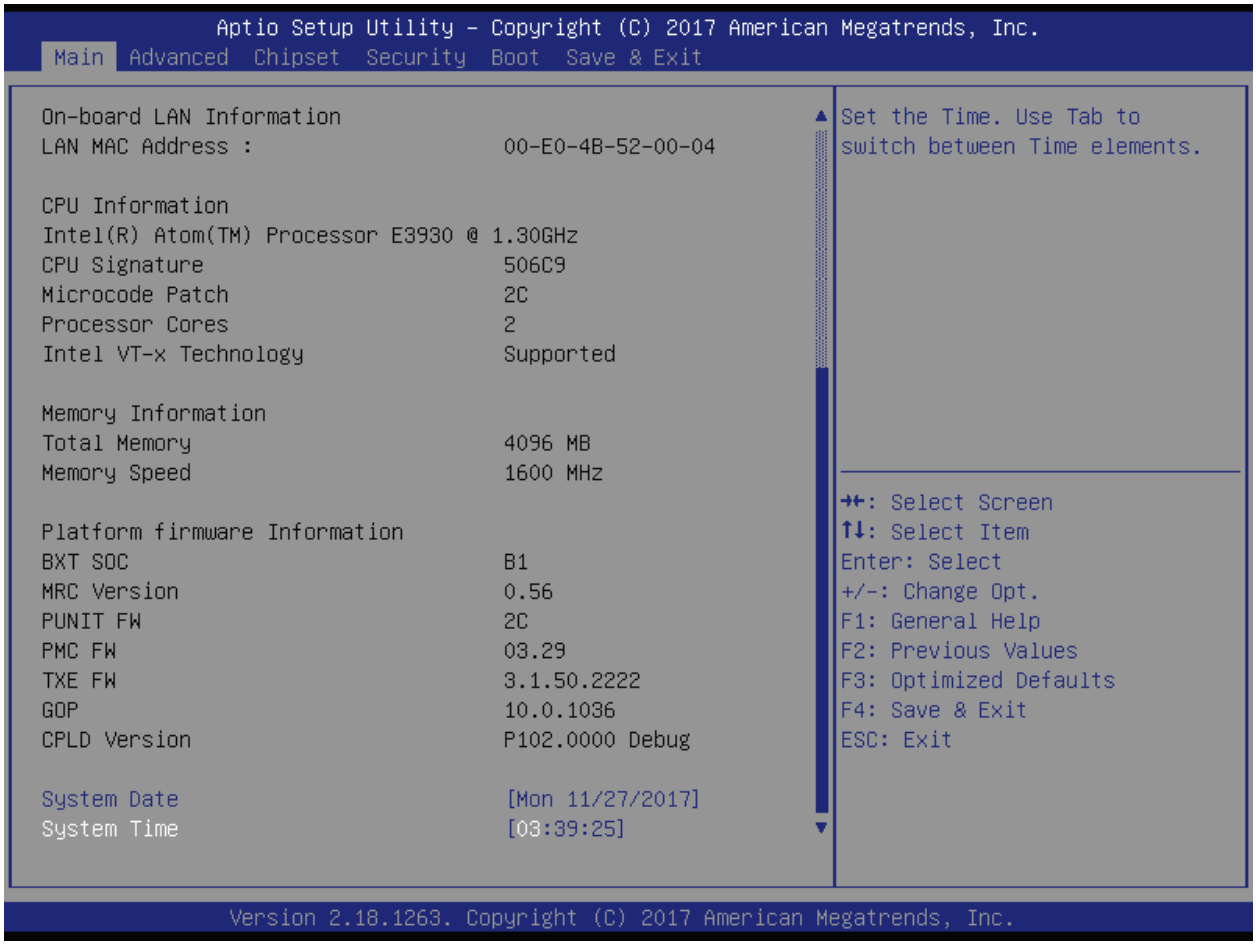
The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Use the left and right arrow keys to select the Setup menus.

Each Setup menu provides two main frames. The left frame displays all available functions. Configurable functions are displayed in blue. Functions displayed in black provide information about the status or the operational configuration. The right frame displays a Help window providing an explanation of the respective function.

7.3. Main Setup Menu

On entering the uEFI BIOS, the Setup program displays the Main Setup menu. This screen lists basic system and board information.

Figure 15: Main Setup Menu Initial Screen



The following table shows Main sub-screens and functions, and describes the content. Default settings are in **bold**.

Table 15: Main Setup Menu Sub-screens

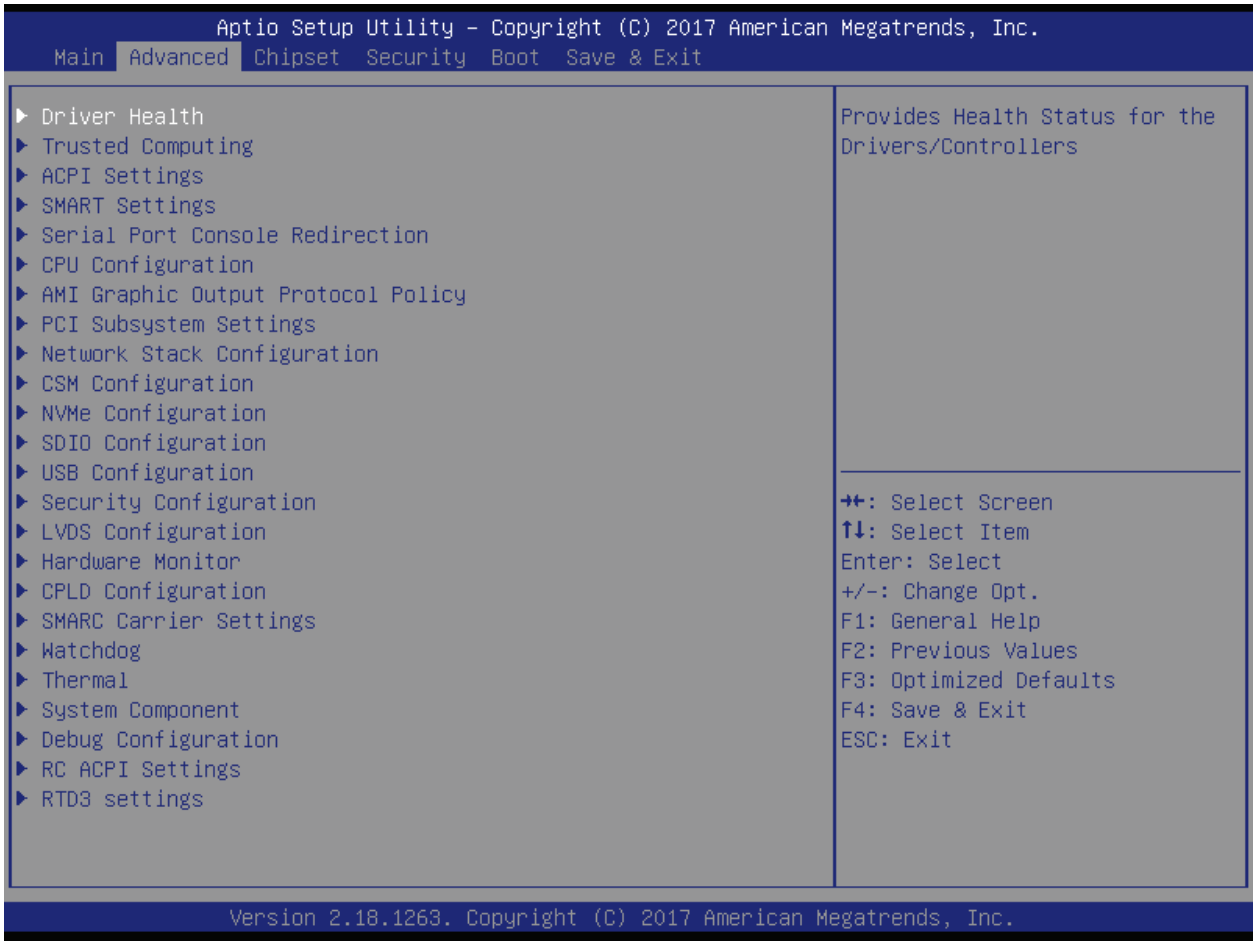
Sub-Screen	Function	Second level Sub-Screen / Description
BIOS Information	Read only field	
	Displays BIOS Information	
	Board Vendor, BIOS Version, Build Date and Time, Access Level	
Board Information	Read only field	
	Displays Board Information	
	Manufacturer, Product Name, PCB Version, Serial Number, Part Number, Boot Count	
On-board LAN Information	Read only field	
	Displays LAN MAC Address	
CPU Information	Read only field	
	Displays CPU Information	
Memory Information	Read only field	
	Displays Memory Information	
Platform firmware Information	Read only field	
	Displays Platform firmware Information	
System Date>	Sets the system date	
	[mm/dd/yyyy]	
System Time>	Sets the system time	
	[hh:mm:ss]	

7.4. Advanced Setup Menu

The Advanced Setup menu provides sub-screens and second level sub-screens with functions, for advanced configuration and Kontron specific configurations.

NOTICE Setting items, on this screen, to incorrect values may cause system malfunctions.

Figure 16: Advanced Setup Menu Initial Screen



The following table shows the Advanced sub-screens and functions and describes the content. Default settings are in **bold** and some functions include additional information. The function / submenu in *italic* indicate either status display or submenu string that cannot be selected. The underlined statement indicates the condition for the availability of the second-level submenu in reference to submenu.

Table 16: Advanced Setup menu Sub-screens and Functions

Sub-Screen	Function	Second level Sub-Screen / Description
Driver Health	*Intel® PRO/1000 7.0.06 PCI-E*	
Trusted Computing	*TPM20 Device Status, Vendor and Firmware Version.* Security Device Support **[Enable]**	<u>When set to Enable:</u> *Active PCR banks* *Available PCR banks*
		SHA-1 PCR Bank **[Enabled]**
		SHA256 PCR Bank **[Enabled]**
		Pending operation **[None]**
		Platform Hierarchy **[Enabled]**
		Storage Hierarchy **[Enabled]**
		Endorsement Hierarchy **[Enabled]**
		TPM2.0 UEFI Spec Version **[TCG_2]**
		Physical Presence Spec Version **[1.3]**
		TPM 20 InterfaceType [TIS]
		Device Select **[Auto]**
ACPI Settings	Enable ACPI Auto Configuration **(Disabled)**	<u>When set to Disable:</u> Enable Hibernation **[Enabled]** ACPI Sleep State **[S3 (Suspend to RAM)]** Lock Legacy Resources **[Disabled]**
SMART Settings	SMART Self Test **[Disabled]**	
Serial Port Console Redirection	Console Redirection (COM0, COM1, COM2, COM3) > **[Disabled]**	<u>When set to Enabled:</u> COM# Console Redirection Settings **[ANSI]** Bits per second **[115200]** Data Bits **[None]** Stop Bits **[1]** Flow Control **[None]** VT-UTF8 Combo Key Support **[Enabled]** Recorder Mode **[Disabled]** Resolution 100x31 **[Disabled]** Legacy OS Redirection Resolution **[80x24]** Putty KeyPad **[VT100]** Redirection After BIOS POST **[Always Enable]**
	Legacy Console Redirection Settings >	Legacy Serial Redirection Port **[COM0]**
	Serial Port for Out-of-Band Management / Windows Emergency	<u>When set to Enabled:</u> Console Redirection Settings > Out-of-Band Mgmt Port **[COM0]** Terminal Type **[VT-UTF8]** Bits per second **[115200]**

Sub-Screen	Function	Second level Sub-Screen / Description
	Management Services (EMS) Console Redirection > **[Disabled]**	Flow Control **[None]** Data Bits **[8]** Parity **[None]** Stop Bits **[1]**
CPU Configuration	Turbo Mode **[Enabled]**	
	Intel Virtualization Technology **[Enabled]**	
	VT-d **[Disabled]**	
	Monitor Mwait **[Disabled]**	
AMI Graphic Output Control Policy	*Intel ® Graphics Controller* *Intel ® GOP Driver* Output select **[DP1]**	
PCI Subsystem Settings	*AMI PCI Driver Version* Above 4G Decoding **[Disabled]**	
	Hot-Plug Support **[Enabled]**	
Network Stack Configuration	Network Stack **[Disabled]**	
	CSM Support **[Enabled]**	When set to Enabled: *CSM16 Module Version 07.79* GateA20 Active **[Upon Request]** INT19 Trap Response **[Immediate]** Boot option filter **[UEFI and Legacy]** *Option ROM execution* Network **[UEFI]** Storage **[UEFI]** Video **[UEFI]** Other PCI devices **[UEFI]**
NVMe Configuration	*NVME controller and Drive information*	
SDIO Configuration	SDIO Access Mode **[Auto]** *Mass Storage Devices:*	
USB Configuration	Legacy USB Support **[Enabled]**	
	XHCI Hand-off **[Enabled]**	
	USB Mass Storage Driver Support **[Enabled]**	
	USB transfer time-out **[20 sec]**	
	Device reset time-out **[20 sec]**	

Sub-Screen	Function	Second level Sub-Screen / Description
	Device power-up delay **[Auto]**	
Security Configuration	TXE HMRFPO **[Disabled]**	
	TXE EOP Message **[Enabled]**	
LVDS Configuration	LVDS Flat Panel Display Support **[Disabled]**	When set to Enabled: Panel Type **[Standard]** Resolution **[1024 x 768]** Panel Color Depth **[24-Bit VESA]** Channel **[Dual]** Bus Swapping **[Swapped]** Clock Frequency Center Spread **[Disabled]** Differential Output Swing Level **[300 mV]** Backlight Signal **[Active High]** Backlight PWM Frequency **[200 Hz]** Brightness Level **[80%]**
Hardware Monitor	*Hardware Monitoring:* *CPU DTS Temperature (CPU MSR)* *PCB Temperature (TD1)* *NCT7802Y Temperature (LTD)* *NCT7802Y Voltage (VCC)* *RTC Voltage (VCORE)* *DDR Voltage (VSENS2)* *Input Voltage (VSENS3)*	
	CPU Fan: CPU Fan Pulse CPU Fan Control Mode **[SMART FAN IV]** Fan Trip Point Trip Point Speed	
	System Fan: System Fan Pulse System Fan Control Mode **[SMART FAN IV]** Fan Trip Point Trip Point Speed	
CPLD Configuration	Serial Port 0 **[Enabled]**	When set to Enabled: Base Address **[3E8]** IRQ **[10]**
	Serial Port 1 **[Enabled]**	When set to Enabled: Base Address **[2E8]** IRQ **[11]**
	GPIO IRQ **[Disabled]**	
	I2C IRQ **[Disabled]**	
	GPIO MUX0 Select **[GPIO0+GPIO2 Enabled]**	
	GPIO MUX1 Select **[GPIO1+GPIO3 Enabled]**	
	GPIO MUX2 Select **[HDA Audio Enabled]**	

Sub-Screen	Function	Second level Sub-Screen / Description
	GPIO MUX3 Select **[FAN Control Enabled]**	
SMARC Carrier Settings	SMARC Carrier I2C0 / SMBUS **[Use I2C0 Controller]**	
	Lid Switch Mode **[Enabled]**	
	Sleep Button Mode **[Enabled]**	
Watchdog	Auto-reload **[Disabled]**	
	Global Lock **[Disabled]**	
	Stage 1 mode **[Disabled]**	
Thermal	Automatic Thermal Reporting **[Disabled]**	When set to Disabled: Critical Trip Point **[125 C]** Passive Trip Point **[95 C]** Passive TC1 value 1 Passive TC2 value 5 Passive TSP value 10
System Component	OS Reset Select **[Cold Reset]**	
	Spread Spectrum Clocking Configuration	
	DDR SSC **[Enable]**	When set to Enable: DDR SSC Selection Table **[-0.5%]**
	DDR SSC Bending Selection Table **[0% (No Clock Bending)]**	
	HighSpeed SerialIO SSC **[Enable]**	When set to Enable: HighSpeed SerialIO SSC Selection Table **[-0.5%]**
Debug Configuration	*Kernel Debugger Configuration* Kernel Debugger Enable **[Disabled]**	
	APEI BERT Configuration APEI BERT **[Enable]**	
	ACPI Memory Debug Switch ACPI Memory Debug **[Disable]**	
	TXE Debug Option End of Post **[Disable]** Lock Directory **[Disable]**	
	PTT Debug Option Suppress PTT Commands **[Disable]**	
	TDO GPIO Pin Switch TDO GPIO Pin **[Enable]**	

Sub-Screen	Function	Second level Sub-Screen / Description
	Max Memory 2G **[Disable]** Persistent RAM Size **[Disable]**	
	OS DnX OS DnX focus entry **[Disable]**	
	Processor Trace Configuration Processor Trace memory allocation **[Disable]**	
	CSE Data Clear Option CSE Data Clear (Yes / No)	
	Option to clear Data region during IFWI Update Capsule Data Clear **[Enable]**	
	NPK Debug Configuration >	North Peak Enable **[Auto]** FW Trace Enable **[Enable]** FW Trace Destination **[PTI]** NPK Recovery Dump **[Disable]** Memory Region 0 Buffer Size **[None]** Memory Region 0 Buffer WrapAround **[Wrap]** Memory Region 1 Buffer Size **[None]** Memory Region 1 Buffer WrapAround **[Wrap]** PTI Mode **[X4]** PTI Training **[Off]** PTI Speed **[Quarter Speed]** Punit Message Level **[LEVEL LOW]** PMC Message Level **[LEVEL LOW]**
RC ACPI Settings	Native PCIE Enable **[Enable]**	
	Native ASPM **[Enable]**	
RTD3 Settings	RTD3 Support **[Disable]**	

7.5. Chipset Setup Menu

The Chipset Setup menu provides sub-screens, second level and third level sub-screens with functions, for Intel Chipset configurations.

Figure 17: Chipset Setup Menu Initial Screen

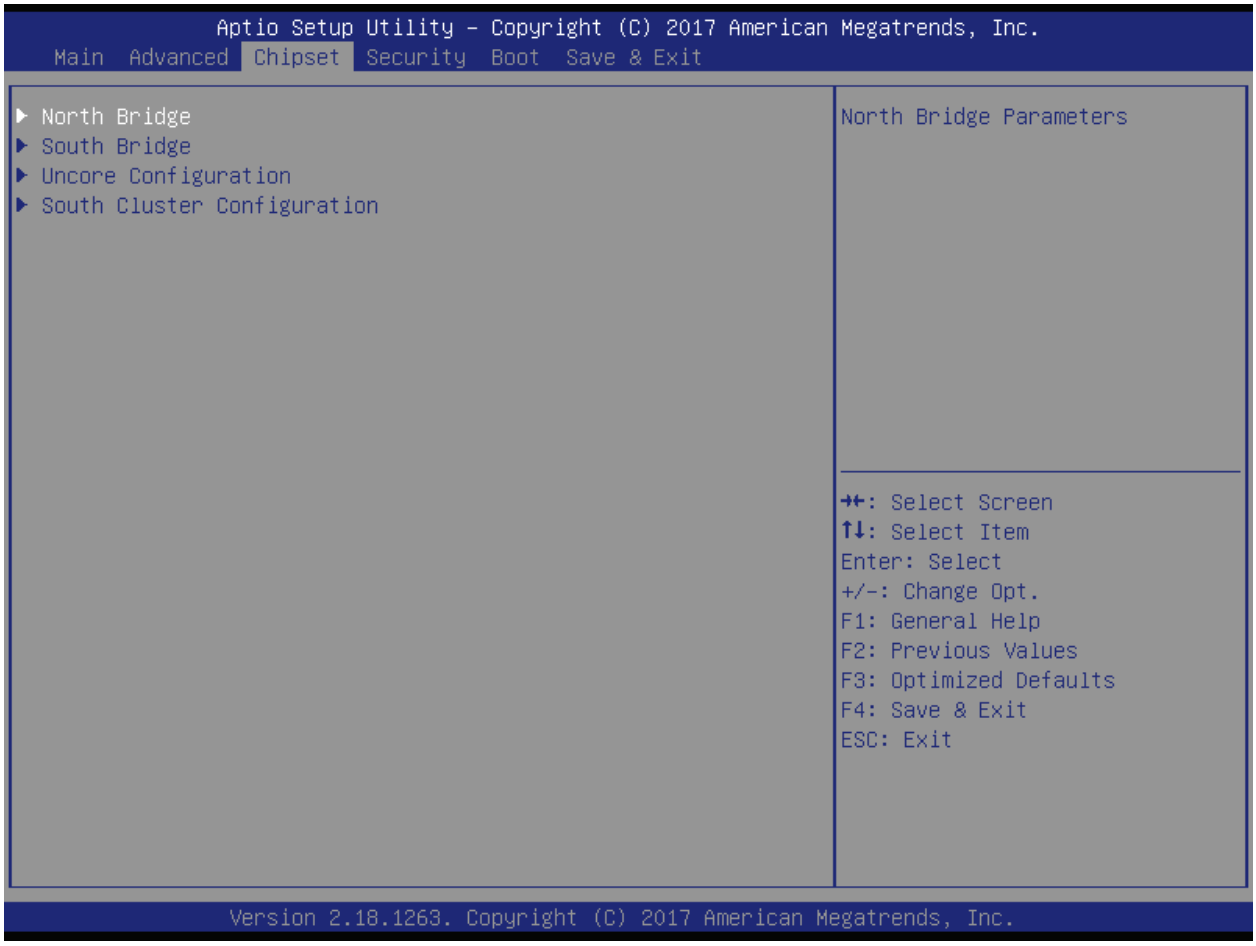


Table 17: Chipset Setup menu Sub-screens and Functions

Sub-Screen	Function	Second level Sub-Screen / Description
North Bridge	Max TOLUD **[2 GB]**	
	PCIE VGA Workaround **[Disable]**	
South Bridge	Serial IRQ Mode **[Continuous]**	
	SMBus Support **[Enabled]**	
	OS Selection **[Windows 10 (Ver>=167)]**	
	PCI Clock Run **[Enable]**	
	Real Time Option **[RT Disable]**	
Uncore Configuration	*GOP Configuration*	
	GOP Driver **[Enable]**	
	Intel Graphics Pei Display PEIM **[Disable]**	
	GOP Brightness Level **[140]**	

Sub-Screen	Function	Second level Sub-Screen / Description
	VBT Select **[DDI1=DP++/HDMI]**	
	IGD Configuration Integrated Graphics Device **[Enable]** Primary Display **[IGD]** RC6 (Render Standby) **[Disable]** GTT Size **[8MB]** Aperture Size **[256MB]** DVMT Pre-Allocated **[64M]** DVMT Total Gfx Mem **[256M]** Cd Clock Frequency **[624 MHz]** GT PM Support **[Enable]** PAVP Enable **[Enable]**	
	IGD – LCD Control BIA **[Auto]** ALS Support **[Enable]** IGD Flat Panel **[Auto]** IGD Boot Type **[Auto]** Panel scaling **[Auto]** GMCH BLC Control **[PWM-Inverted]**	
	IPU PCI Device Configuration IPU Enable / Disable **[Disable]**	
South Cluster Configuration	*HD-Audio Configuration >*	HD-Audio Support **[Enable]** HD-Audio DSP **[Enable]** Audio DSP Compliance Mode **[UAA (HAD Inbox/IntelSST]** WoV (Wake on Voice) **[Disable]** Bluetooth Sideband **[Enable]** SRAM Reclaim **[Enable]** BT Intel HFP **[Enable]** BT Intel A2DP **[Disable]** Context Aware **[Disable]** DMIC **[Disable]** Bluetooth **[Disable]** *I2S SKP **[Enable]*** *I2S HP **[Enable]*** Codec based VAD **[Disable]** DSP based Speech Pre-Processing **[Disable]** *Voice Activity Detection* **[Intel Wake on Voice]** Waves **[Disable]** DTS **[Disable]** Spatial **[Disable]** Dolby **[Disable]** Samsung SoundAlive **[Disable]** Samsung SoundBooster **[Disable]** Samsung EQ/DRC **[Disable]** ForteMedia SAMSoft **[Disable]** *Intel WoV **[Disable]*** *Sensory WoV **[Disable]***

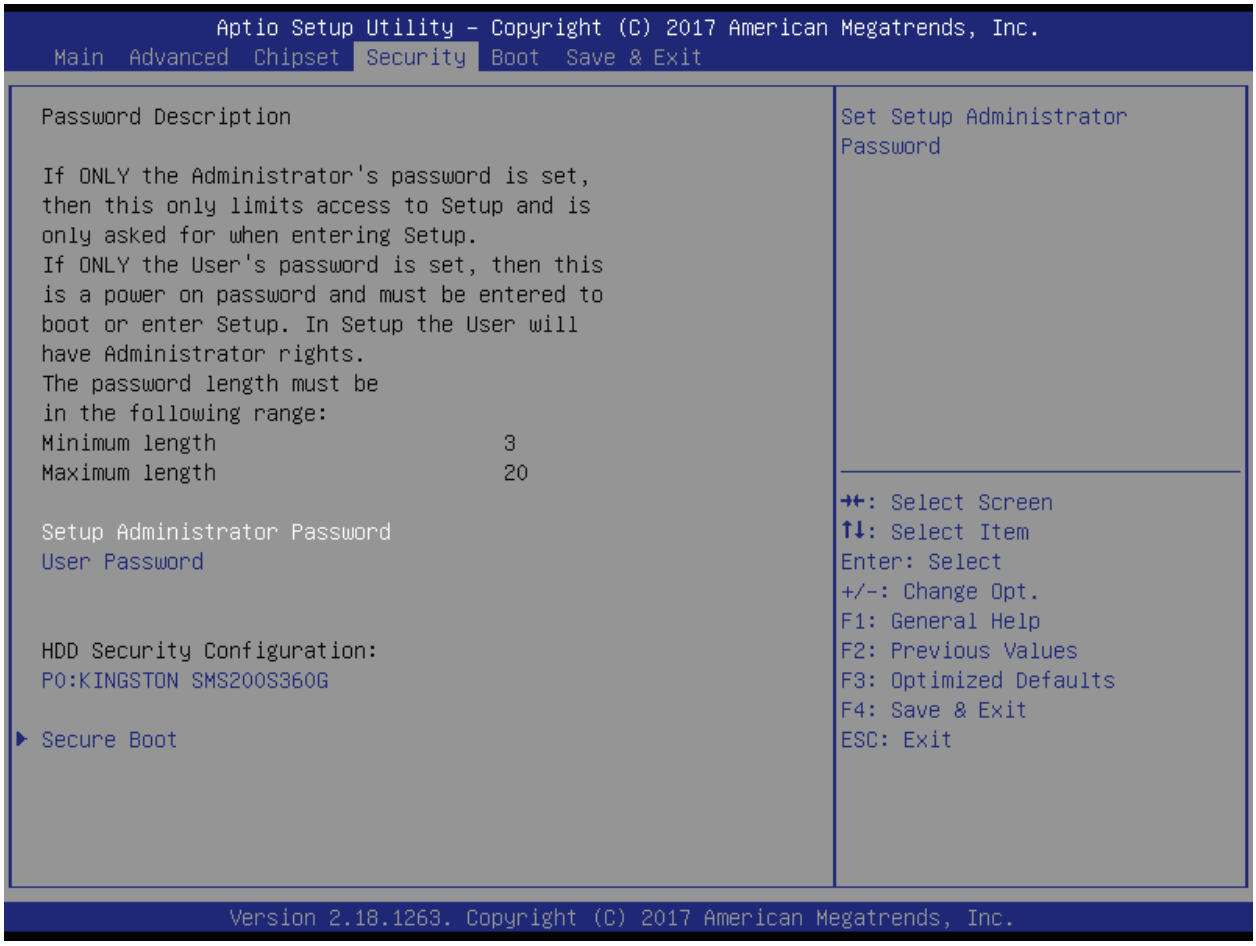
Sub-Screen	Function	Second level Sub-Screen / Description
		Conexant Pre-Process **[Disable]** *Context Aware Pre-Process **[Disable]*** Custom Module 'Alpha' **[Disable]** Custom Module 'Beta' **[Disable]** Custom Module 'Gamma' **[Disable]** HD-Audio CSME Memory Transfers **[VCO]** HD-Audio Host Memory Transfers **[VCO]** HD-Audio I/O Buffer Ownership Selection **[HD-Audio Link owns all the I/O buffers]** HD-Audio Clock Gating **[Enable]** HD-Audio Power Gating **[Enable]** HD-Audio PME **[Enable]** HD-Audio Link Frequency **[24 MHz]** iDisplay Link Frequency **[96 MHz]**
	LPSS Configuration >	*Low Power Sub System* LPSS I2C1 Support (D22:F1) **[Enable]** LPSS I2C2 Support (D22:F2) **[Enable]** LPSS I2C3 Support (D22:F3) **[Enable]** LPSS I2C4 Support (D23:F0) **[Enable]** LPSS HSUART1 Support (D24:F1) **[Enable]** LPSS HSUART2 Support (D24:F2) **[Enable]** LPSS SPIO Support (D25:F0) **[Enable]** LPSS IOSF PMCTL SOix Enable **[Enable]**
	PCI Express Configuration >	*PCI Express Configuration* PCI Express Clock Gating **[Enable]** Port8xh Decode **[Disable]** Peer Memory Write Enable **[Disable]** Compliance Mode **[Disable]** > PCIe #4 BDF[00:14:00] > PCIe #5 NC > PCIe #0 BDF[00:13:00] > PCIe #1 BDF[00:13:01] > PCIe #2 BDF[00:13:02] > PCIe #3 BDF[00:13:03] <u>When PCIE #X is enabled:</u> PCIe #X BDF[XX:XX:XX] **[Auto]** ASPM **[Disable]** L1 Substates **[L1.1 & L1.2]** ACS **[Enable]** URR **[Disable]** FER **[Disable]** NFER **[Disable]** CER **[Disable]** CTO **[Default Setting]** SEFE **[Disable]** SENFE **[Disable]**

Sub-Screen	Function	Second level Sub-Screen / Description
		SECE **[Disable]** PME SCI **[Enable]** Hot Plug **[Disable]** PCIE Speed **[Auto]** Transmitter Half Swing **[Disable]** *Extra Bus Reserved 0* *Reserved Memory 10* *Reserved I/O 4* PCH PCIE LTR **[Enable]** Snoop Latency Override **[Auto]** Non Snoop Latency Override **[Auto]** PCIE LTR Lock **[Disable]** PCIE Selectable De-emphasis **[Enable]**
	SATA Drives >	*SATA Drives* *Chipset-SATA Controller Configuration* SATA Test Mode **[Disable]** *SATA Port 0* Port 0 **[Enable]** SATA Port 0 Hot Plug Capability **[Disable]**
	SCC Configuration >	SCC SD Card Support (D27:F0) **[Enable]** SCC eMMC Support (D28:F0) **[Enable]** eMMC Max Speed **[HS200]**
	USB Configuration >	USB Port Disable Override **[Disable]** XDCI Support **[Disable]** XHCI Disable Compliance Mode **[FALSE]** USB HW MODE AFE Comparators **[Disable]**
	Miscellaneous Configuration >	State After G3 **[S0 State]** Power Button Debounce Mode **[Enable]** Wake on LAN **[Disable]** BIOS Lock **[Disable]** RTC Lock **[Enable]** TCO Lock **[Disable]** DCI Enable (HDCIEN) **[Disable]** DCI Auto Detect Enable **[Enable]** GPIO Lock **[Disable]**

7.6. Security Setup Menu

The Security Setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive.

Figure 18: Security Setup Menu Initial Screen



The following table shows Security sub-screens and functions.

Table 18: Security Setup Menu Functions

Function	Description
Setup Administrator Password User Password	Create / change password to enter Setup
HDD Security Configuration	Create / change password to allow access to Set, Modify and Clear HardDisk User and Master Passwords for Enabling Security.
Attempt Secure Boot **[Disable]**	Enable or Disable the Secure Boot support. Please also set Secure Boot Mode to "Standard" to install standard Microsoft Platform Key (PK).
Secure Boot Mode	Set Secure Boot Mode to "Standard" to boot standard Windows or Linux boot loader signed with Microsoft's platform key. Select "Customized" mode only if you have a custom OS with OS boot loader signed with your own platform key. Kontron provide services for Customized Secure Boot, visit Kontron SEC-Line home page https://www.kontron.com/products/solutions/security/sec-line.html for more information.
Key Management	Enables expert users to modify Secure Boot Policy Variables without full authentication.

If only the administrator's password is set, then only access to the setup is limited and is requested when entering the setup.

If the user's password is set, then the password is a power on password and must be entered to boot or enter setup. In the setup the user has restricted rights.

7.6.1. Remember the Password

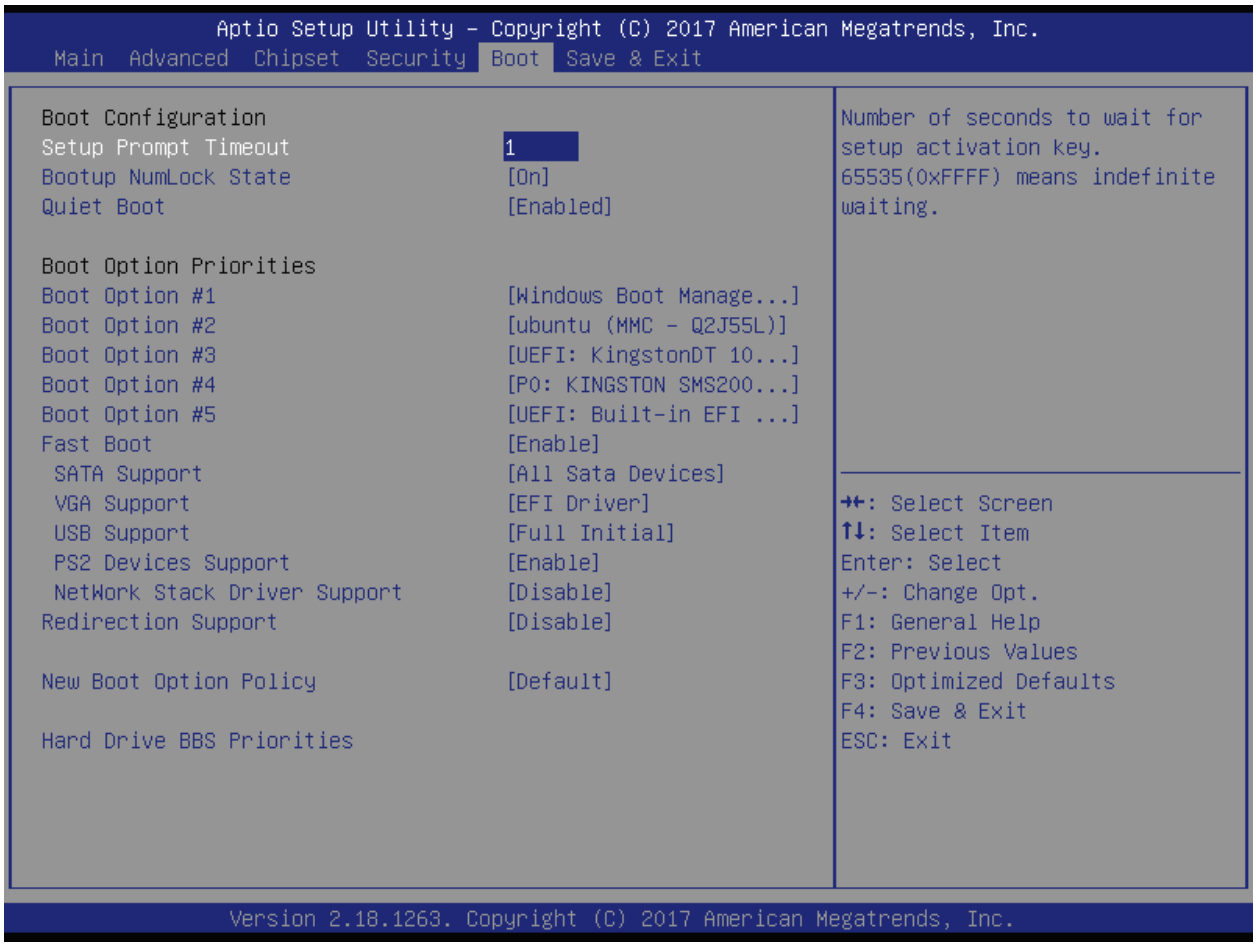
It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords result in the user being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not known, contact Kontron Support for further assistance.

7.7. Boot Setup Menu

The Boot Setup menu lists dynamically generated boot device priority order.

Figure 19: Boot Setup Menu Initial Screen



The following table shows Boot sub-screens and functions, and describes the content. Default settings are in **bold**.

Table 19: Boot Setup Menu Functions

Function	Description
Boot Configuration Setup Prompt Timeout **1** Bootup NumLock State **[On]** Quiet Boot **[Enabled]**	
Boot Option Priorities Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4 Fast Boot **[Enable]** SATA Support VGA Support USB Support	To set the system boot order. Use +/- keys to change option. When Fast Boot is Enabled, SATA, VGA, USB, PS2 support, devices initialization, Network Stack driver can be customized.

Function	Description
PS2 Support Network Stack Driver Support Redirection Support	
New Boot Option Policy	Controls the placement of newly detected UEFI boot options
Hard Drive BBS Priotities	Sets the placement of legacy boot options

Boot options for the SMARC-sXAL (BOOT_SEL2#):

Only boot from module BIOS or carrier BIOS supported, no other boot options supported.

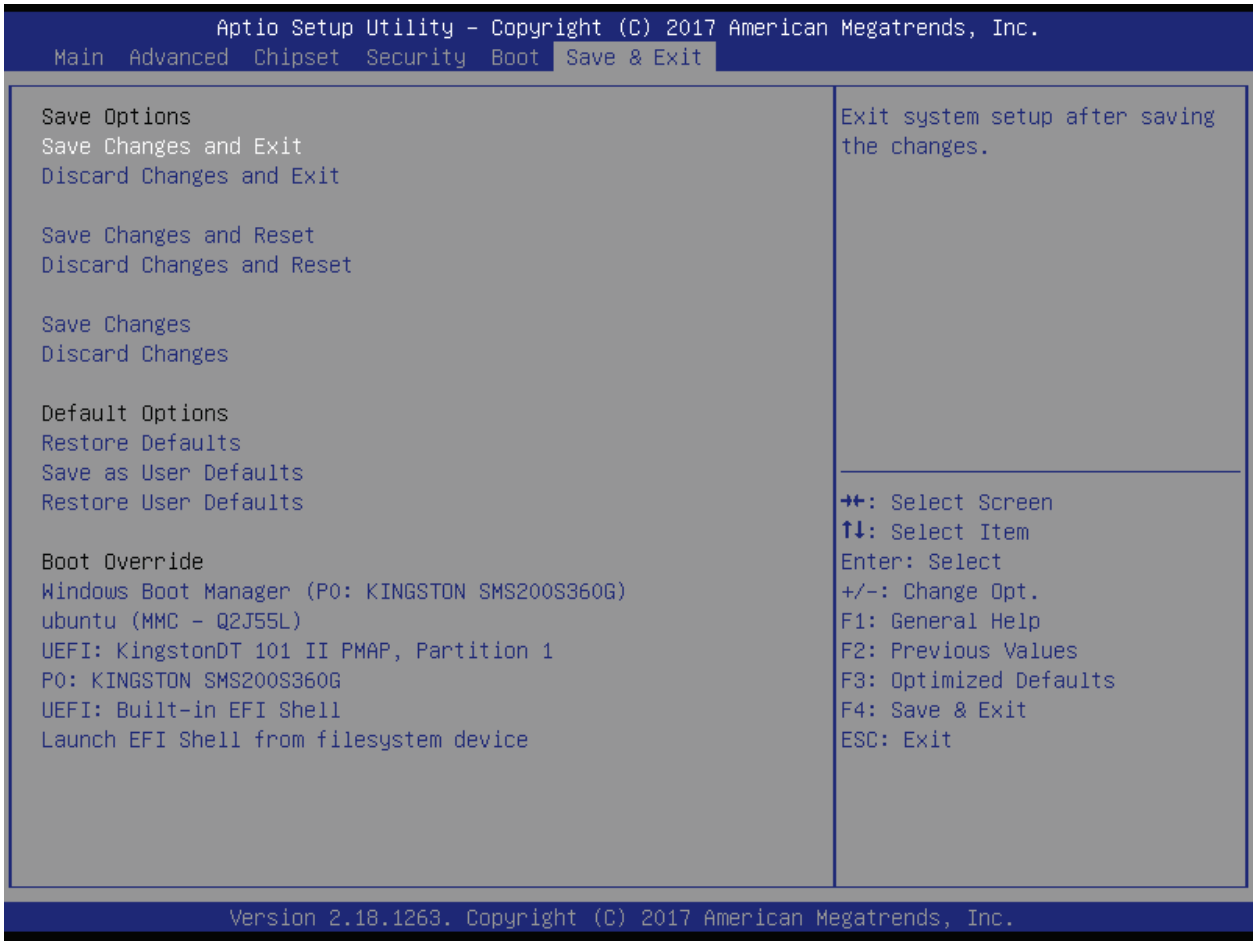
- To boot from module, remove shunt jumper on J33 (BOOT_SEL2#) of SMARC-EVAL V2.0 carrier.
- To boot from carrier, place shunt jumper on J33 (BOOT_SEL2#) of SMARC-EVAL V2.0 carrier.

7.8. Exit Setup Menu

The Save and Exit Setup menu provides functions for handling changes made to the uEFI BIOS settings and exiting the Setup program.

If system cannot boot or work properly due to incorrect setting, activating the Force Recovery jumper will load the default setting of BIOS upon power cycle. Please check with your SMARC Carrier System provider for more information. Once safely booted with default setting, you may deactivate the Force Recovery jumper to save new changes on BIOS setting.

Figure 20: Save and Exit Setup Menu Initial Screen



The following table shows the Exit menu sub-screens and functions, and describes the content.

Table 20: Save and Exit Setup Menu Functions

Function	Description
Save Options Save Changes and Exit Discard Changes and Exit Save Changes and Reset Discard Changes and Reset Default Options Restore Defaults Save as User Defaults Restore User Defaults	
Boot Override UEFI: Built-in EFI Shell Launce EFI Shell from filesystem device	

7.9. The uEFI Shell

The Kontron uEFI BIOS features a built-in and enhanced version of the uEFI Shell. For a detailed description of the available standard shell scripting, refer to the EFI Shell User Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage (http://sourceforge.net/projects/efi-shell/files/documents/).

Kontron uEFI BIOS does not provide all shell commands described in the EFI Shell Command Manual. If Secure Boot is enabled, the UEFI shell may not be able to be entered.

7.10. Basic Operation of the uEFI Shell

7.10.1. Entering the uEFI Shell

To enter the uEFI Shell, follow the steps below:

1. Power on the board.
2. Press the <F7> key (instead of <DEL>) to display a choice of boot devices.
3. Choose 'UEFI: Built-in EFI Shell'.

```
EFI Shell version 2.50 [5.12]
Current running mode 1.1.2
Device mapping table
Fs0        :HardDisk - Alias hd33b0b0b fs0
   Acpi(PNP0A03,0)/Pci(1D|7)/Usb(1, 0)/Usb(1, 0)/HD(Part1,Sig17731773)
Press the ESC key within 5 seconds to skip startup.nsh, and any other key to continue.
```

4. The output produced by the device-mapping table can vary depending on the board's configuration.
5. If the ESC key is pressed before the 5 second timeout elapses, the shell prompt is shown:

```
Shell>
```

7.10.2. Exiting the uEFI Shell

To exit the uEFI Shell, follow one of the steps below:

1. Use the **exit** uEFI Shell command to select the boot device, in the Boot menu, that the OS will boot from.
2. Reset the board using the **reset** uEFI Shell command.

7.11. uEFI Shell Scripting

7.11.1. Startup Scripting

If the ESC key is not pressed and the timeout has run out then the uEFI Shell tries to execute some startup scripts automatically. It searches for scripts and executes them in the following order:

1. Initially searches for Kontron flash-stored startup script.
2. If there is no Kontron flash-stored startup script present then the uEFI-specified **startup.nsh** script is used. This script must be located on the root of any of the attached FAT formatted disk drive.
3. If none of the startup scripts are present or the startup script terminates then the default boot order is continued.

7.11.2. Create a Startup Script

Startup scripts can be created using the uEFI Shell built-in editor edit or under any OS with a plain text editor of your choice. To create a startup shell script, simply save the script on the root of any FAT-formatted drive attached to the system.

7.12. Examples of Startup Scripts

7.12.1. Execute Shell Script on other Harddrive

This example (**startup.nsh**) executes the shell script named **bootme.nsh** located in the root of the first detected disc drive (**fs0**).

```
fs0:
bootme.nsh
```

7.13. Firmware Update

Firmware updates are typically delivered as a ZIP archive containing only the firmware images. The content of the archive with the directory structure must be copied onto a data storage device with FAT partition.

7.13.1. Updating Procedure

BIOS can be updated with the Intel tool fpt64.efi using the procedure below:

1. Copy these files to an USB stick.
   - flash.nsh or flash_with_fpt.nsh (if available)
   - fpt.efi
   - fparts.txt
   - SMARC_sXALi_BIOS_<xxx>……bin (where xxx stands for the version #)
2. Start the system into the uEFI shell (see chapter 7.10.1 “Entering the uEFI Shell”).
3. Change to the drive representing the USB stick.

```
fsx:   (x = 0,1,2,etc. represents the USB stick)
```

4. Change to the directory where you copied the flash tool.

```
cd <your_directory>
```

5. Start flash.nsh or flash_with_fpt.nsh (if available)

   or type

   ```
   fpt -y -f SMARC_sXALi_BIOS_<xxx>……bin
   ```

6. Wait until flashing is successful and then power cycle the board.

Do not switch off the power during the flash process!

8/ Technical Support

For technical support contact our Support department:

E-mail: support@kontron.com
Phone: +49-821-4086-888

Make sure you have the following information available when you call:

Product ID Number (PN),
Serial Number (SN)

The serial number can be found on the Type Label, located on the product's rear side.

Be ready to explain the nature of your problem to the service technician.

8.1. Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law. This applies to the CMOS battery, for example.

If there is a protection label on your product, then the warranty is lost if the product is opened.

8.2. Returning Defective Merchandise

All equipment returned to Kontron must have a Return of Material Authorization (RMA) number assigned exclusively by Kontron. Kontron cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to Kontron's designated facility. Kontron will pay the return freight charges back to the buyer's location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to Kontron.

1. Visit the RMA Information website:
http://www.kontron.com/support-and-services/support/rma-information

   Download the RMA Request sheet for **Kontron Europe GmbH** and fill out the form. Take care to include a short detailed description of the observed problem or failure and to include the product identification Information (Name of product, Product number and Serial number). If a delivery includes more than one product, fill out the above information in the RMA Request form for each product.

2. Send the completed RMA-Request form to the fax or email address given below at Kontron Europe GmbH. Kontron will provide an RMA-Number.

   Kontron Europe GmbH
   RMA Support
   Phone: +49 (0) 821 4086-0

Fax: +49 (0) 821 4086 111
Email: service@kontron.com

3. The goods for repair must be packed properly for shipping, considering shock and ESD protection.

Goods returned to Kontron Europe GmbH in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

4. Include the RMA-Number with the shipping paperwork and send the product to the delivery address provided in the RMA form or received from Kontron RMA Support.

List of Acronyms

CPLD	Complex Programmable Logic Devices
CSI	Camera Serial Interface
eDP	embedded Display Port
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card
ESD	Electrostatic Discharge
GPIO	General-purpose input/output
HDA	High Definition Audio
HDMI	Integrated High Definition Multimedia Interface
I2S	Inter-IC Sound
LPC	Low Pin Count
LPDDR	Low Power DDR
LVDS	Low Voltage Differential Signalling
MIPI	Mobile Industry Processor Interface
pSLC	pseudo Single Level Cell
PEG	PCI Express External
SDIO	Secure Digital Input Output
SMARC	Smart Mobility ARChitecture
SMBus	System Management Bus
SoC	System on Chip
TPM	Trusted Platform Module
UART	Universal Asynchronous Receiver Transmitter

About Kontron – Member of the S&T Group

Kontron is a global leader in Embedded Computing Technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

For more information, please visit: http://www.kontron.com/

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