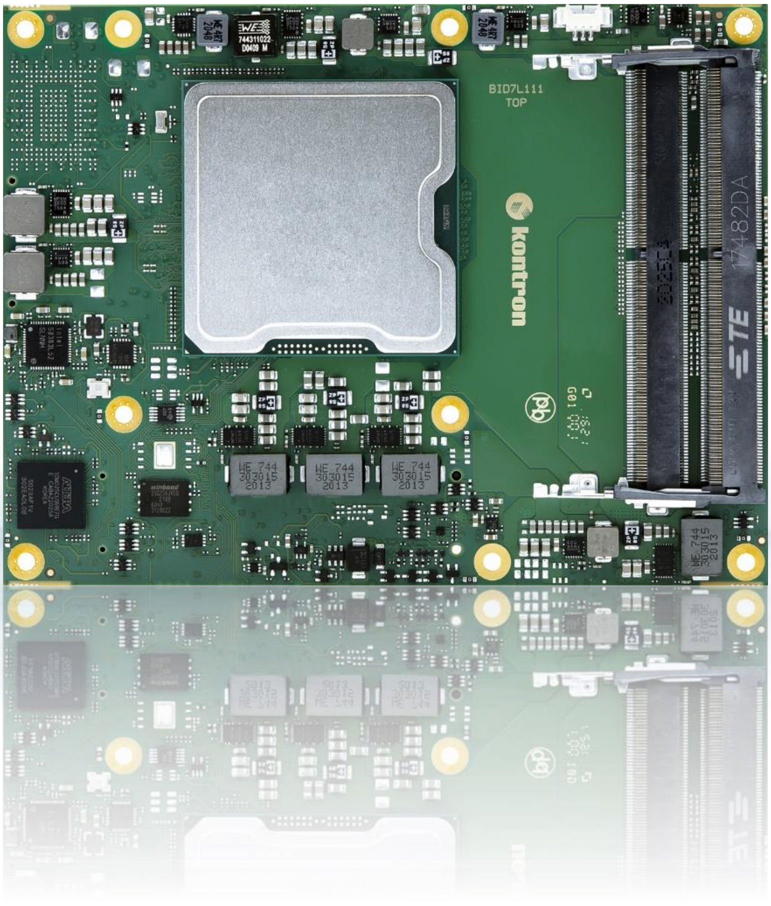
USER GUIDE



COMe-bID7

User Guide Rev. 1.6

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COME-BID7 - USER GUIDE

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⚠CAUTION

Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Please follow the "General Safety Instructions" supplied with the system.

NOTICE

You find the most recent version of the "General Safety Instructions" online in the download area of this product.

NOTICE

This product is not suited for storage or operation in corrosive environments, in particular under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact Kontron Support.

Revision History

Revision	Brief Description of Changes	Date of Issue	Author
1.0	Release	2023-January-24	ih
1.1	Added chapter 3.12	2023-February-08	ih
1.2	New Kontron logo	2023-March-29	ih
1.3	UART option removed	2023-April-19	ih
1.4	Updated chapter 6.5 / 6.6	2023-August-31	ih
1.41	Minor enhancements regarding chapter 6.5 / 6.6	2023-September-18	ih
1.5	Corrected memory P/N, added modified signal names for GBE0 changed with COM.0 Rev3.1	2023-November-24	ih
1.6	Extended CPU-list with IceLake-D refresh SKUs	2024-February-16	ih

Terms and Conditions

Kontron warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit http://www.kontron.com/terms-and-conditions.

Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit http://www.kontron.com/terms-and-conditions.

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

Customer Support

Find Kontron contacts by visiting: https://www.kontron.com/support-and-services.

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

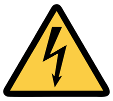
For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit https://www.kontron.com/de/support-and-services/

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this manual

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit http://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.
Kontron follows the WEEE directive
You are encouraged to return our products for proper disposal.

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1/ Introduction

1.1. Product Description

Kontron's Computer-on-Module COMe-bID7 is a COM Express® BASIC TYPE 7 form-factor with Intel®'s Xeon® D-1700/D-1800 processor family. The Intel® Xeon ® D-1700/D-1800 Generation increases efficiency and performance per watt ratio, which is a result of the innovative 10nm technology and has up to 10 cores for control, micro server, storage and communication applications in Internet of Things (IoT) and embedded environment. The COMe-bID7 is also designed for industrial temperature environment.

- Intel® Xeon® Processor D-1700/D-1800 System on Chip (SoC), member of the Intel® Xeon® Processor family
- DDR4 memory technology up to 128 GByte ECC with 4x SODIMM sockets
- High-speed connectivity 16x PCIe Gen4 + 16x PCIe Gen3
- Quad 10 GbE interfaces

1.2. Product Naming Clarification

COM Express® defines a Computer-on-Module, or COM, with all the components necessary for a bootable host computer, packaged as a super component. The product name for Kontron COM Express® Computer-On-Modules consists of:

Industry standard short form

- COMe-

Module form factor

- b=basic (125mm x 95mm)
- c=compact (95mm x 95mm)
- m=mini (84mm x 55mm)

Intel's processor code name

- ID = Ice Lake-D

Pinout type

- 7 = Type 7

Available temperature variants

- Commercial
- E2 = Industrial

Processor Identifier

- Chipset identifier (if chipset assembled)

Storage

- NVMe (if assembled)

1.3. Understanding COM Express® Functionality

All Kontron COM Express® basic and compact modules contain two 220pin connectors; each of it has two rows called Row A & B on primary connector and Row C & D on secondary connector. The COM Express® Computer-On-Module (COM) features the following maximum amount of interfaces according to the PCI Industrial Computer Manufacturers Group (PICMG) module Pin-out type.

Table 1: Pin Assignment of Type 7 and COMe-bID7

Feature	Type 7 Standard	COMe-bID7 Pinout
NBASE-T LAN	1x 10GBit max.	1x 2.5GBit max
10GBASE-KR LAN Ports	4x	4x
NC-SI	1x	1x
PCI Express	32x	16x PCIe Gen3 16x PCIe Gen4
Serial ATA	2x	2x
USB	4x USB 3.2 (USB 2.0)	4x USB 3.1 Gen1 respect. USB 3.0 (USB 2.0)
Serial Ports	2x	2x
eSPI/LPC	1x	1x
External SPI	1x	1x
External SMB	1x	1x
External I2C	1x	1x
GPIO	8x	8x

1.4. COM Express® Documentation

The COM Express® Specification defines the COM Express® module form factor, pin-out, and signals. This specification is available at the PICMG® website by filling out the order form.

1.5. COM Express® Benefits

COM Express® defines a Computer-On-Module, or COM, with all the components necessary for a bootable host computer, packaged as a highly integrated computer. All Kontron COM Express® modules are very compact and feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each COM is based on the COM Express® specification. This standardization allows designers to create a single-system baseboard that can accept present and future COM Express® modules.

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application, on a baseboard optimally designed to fit a system's packaging.

A single baseboard design can use a range of COM Express® modules with different sizes and pinouts. This flexibility differentiates products at various price and performance points and provides a built-in upgrade path when designing future-proof systems. The modularity of a COM Express® solution also ensures against obsolescence when computer technology evolves. A properly designed COM Express® baseboard can work with several successive generations of COM Express® modules.

A COM Express® baseboard design has many advantages of a customized computer-board design and, additionally, delivers better obsolescence protection, heavily reduced engineering effort, and faster time to market.

2/ Product Specification

2.1. Module Definition

The COM Express® basic sized Computer-on-Module COMe-bID7 follows pin-out Type 7 and is compatible to the PICMG specification COM.0 Rev 3.1.

The COMe-bID7 can also be offered compliant to COM-Express Spec Rev 3.0 on request.

The COMe-bID7 is available in different variants to cover the individual demands in performance, price and power.

2.2. Commercial Grade Modules

The following is a list of modules for commercial temperature range.

Table 2: Commercial Grade Modules (0°C to 60°C operating)

Product Number	Product Name	Description
68008-0000-49-2	COMe-bID7 D-1749NT	COM Express® basic pin-out type 7 COM.0 R3.1 with Intel®D-1749NT, 90 W, 10 core, 3.0 GHz, 4x 10GBASE-KR, 16x PCIe Gen4, 16x PCIe Gen3, 2x DDR4 SO-DIMM socket
68008-0000-35-1	COMe-bID7 D-1735TR	COM Express® basic pin-out type 7 COM.0 R3.1 with Intel® D-1735TR, 59 W, 8 core, 2.2 GHz, 4x 10GBASE-KR, 4x 10GBASE-KR, 16x PCIe Gen4, 16x PCIe Gen3, 2x DDR4 SO-DIMM socket
68008-0000-12-1	COMe-bID7 D-1712TR	COM Express® COM.0 R3.1 basic pin-out type 7 with Intel® D-1712TR, 40 W, 4 core, 2.0 GHz, 4x 10GBASE-KR, 16x PCIe Gen4, 16x PCIe Gen3, 2x DDR4 SO-DIMM socket

2.3. Industrial Grade Modules

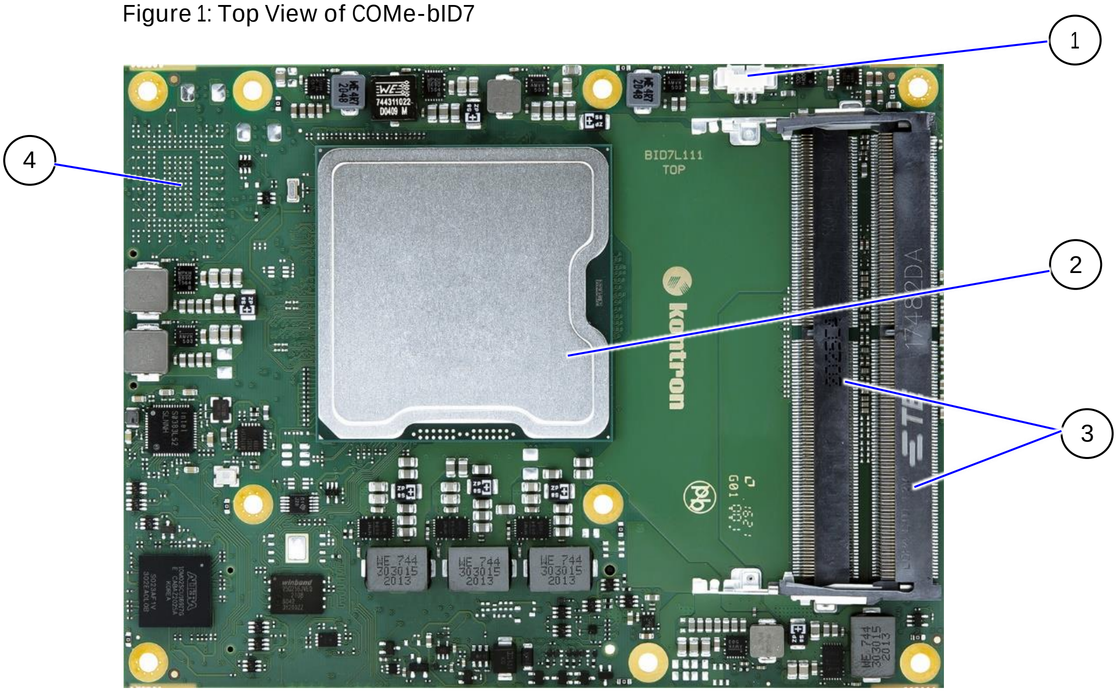
Industrial temperature grade modules are available based on their design. Please contact your local sales or support for further details.

Table 3: Industrial Grade Modules by Design (E2, -40°C up to 85°C Operating)

Product Number	Product Name	Description
68009-0000-46-1	COMe-bID7 E2 D-1746TER	COM Express® basic pin-out type 7 COM.0 R3.1 with Intel® D-1746TER, 67/56 W, 10 core, 2.0 GHz, 4x 10GBASE-KR, 16x PCIe Gen4, 16x PCIe Gen3, 2x DDR4 SO-DIMM socket, industrial temperature
68009-0000-32-1	COMe-bID7 E2 D-1732TE	COM Express® basic pin-out type 7 COM.0 R3.1 with Intel® D-1732TE, 52 W, 8 core, 1.9 GHz, 4x 10GBASE-KR, 16x PCIe Gen4, 16x PCIe Gen3, 2x DDR4 SO-DIMM socket, industrial temperature
68009-0000-15-1	COMe-bID7 E2 D-1715TER	COM Express® basic pin-out type 7 COM.0 R3.1 with Intel® D-1715TER, 50 W, 4 core, 2.4 GHz, 4x 10GBASE-KR, 16x PCIe Gen4, 16x PCIe Gen3, 2x DDR4 SO-DIMM socket, industrial temperature

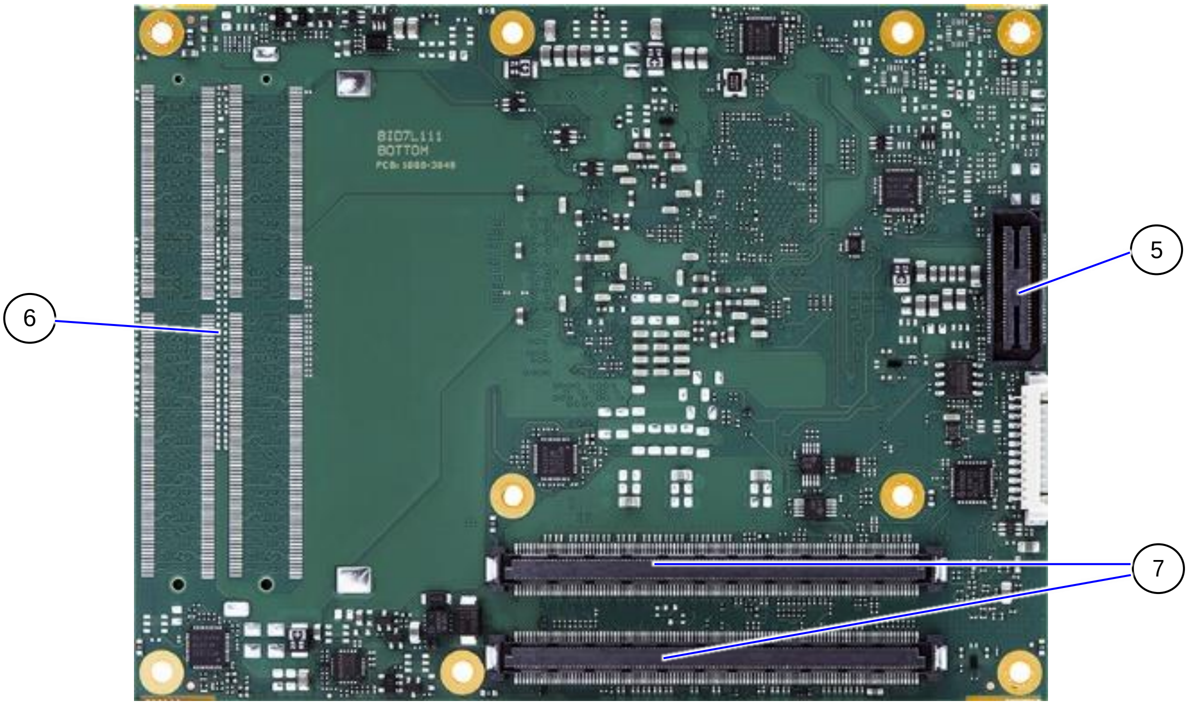
2.4. Product Views

Figure 1: Top View of COMe-bID7



1. Fan Connector
2. Processor
3. 2x DDR4 SODIMM sockets
4. Optional NVMe

Figure 2: Bottom View of COMe-bID7

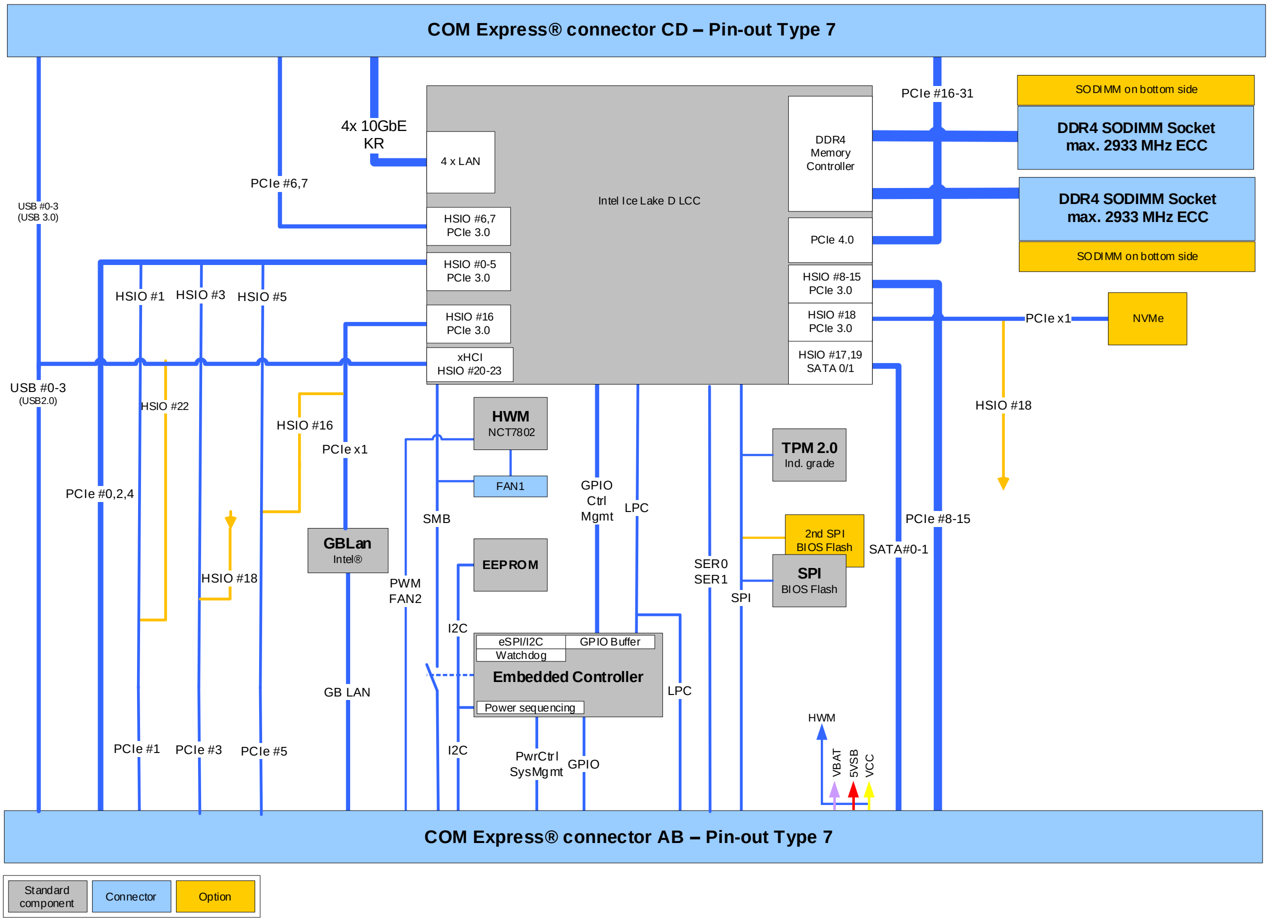


5. XDP debug port (not populated on production units)
6. Optional 2x DDR4 SODIMM sockets
7. 2x COMe connectors

3/ Functional Specification

3.1. Block Diagram COMe-bID7

Figure 3: Block Diagram COMe-bID7



3.2. Processors

The Intel® Xeon® processor D-1700/D-1800 processor family with 45 mm x 45 mm package size (FCBGA) is the next generation System-on-Chip (SoC) with processor cores built using Intel 10-nanometer process technology. The three major complexes in this highly-integrated SoC are the CPU, PCH and NAC. The Central Processing Unit (CPU) complex contains up to 10 next-generation 64-bit processor cores.

The Platform Controller Hub (PCH) of the SoC is architected with a rich set of interconnect technologies.

The Network Accelerator Complex (NAC) includes technologies for security and packet processing.

The SoC architecture is highly scalable and efficient, providing a unified solution across an array of products. The processor SKUs are targeted for long life supply availability with extended reliability in communications environments.

Table 4: Intel® Processor D-1700/D-1800 Product Family Specifications

Intel SKU	SKU	Group	TDP (W)	No. of Cores	IOTG	E-Tmp	Tcase min (°C)	DDR Freq. (MHz)	Base Freq. (GHz)	All/ Max Turbo (GHz)	BW LAN (GbE)	BW QAT (GbE)
D-1746TER	std	NIC	67/56	10	Yes	Yes	-40	2667	2.0	2.5/3.1	100G	OFF
D-1848TER	req	NIC	57	10	Yes	Yes	-40	2667	2.0	2.5/3.1	100G	OFF
D-1749NT	std	QAT	90	10	No	No	0	2667	3.0	3.5/3.5	100G	20G
D-1748TE	req	NIC	65	10	No	Yes	-40	2400	2.3	2.8/3.4	50G	OFF
D-1747NTE	std	QAT	80	10	No	Yes	-40	2933	2.5	3.0/3.5	100G	20G
D-1844NT	std	QAT	55	10	No	No	0	2667	2.0	2.6/3.1	50G	20G
D-1735TR	std	NIC	59	8	Yes	No	0	2933	2.2	2.7/3.4	50G	OFF
D-1732TE	std	NIC	52	8	Yes	Yes	-40	2667	1.9	2.4/3.0	50G	OFF
D-1734NT	req	QAT	50	8	No	No	0	2667	2.0	2.5/3.1	50G	20G
D-1736NT	req	QAT	67	8	No	No	0	2667	2.7	3.2/3.5	50G	20G
D-1733NT	req	QAT	53	8	No	No	0	2400	2.0	2.5/3.1	50G	20G
D-1823NT	req	QAT	55	6	No	No	0	2400	2.8	3.3/3.5	50G	10G
D-1715TER	std	NIC	50	4	Yes	Yes	-40	2667	2.4	2.9/3.5	50G	OFF
D-1712TR	std	NIC	40	4	Yes	No	0	2400	2.0	2.5/3.1	50G	OFF
D-1718T	std	NIC	46	4	No	No	0	2933	2.6	3.1/3.5	50G	OFF
D-1713NT	req	QAT	45	4	No	No	0	2400	2.2	2.9/3.5	50G	10G
D-1713NTE	req	QAT	45	4	No	Yes	-40	2400	2.2	2.7/3.3	50G	10G

D-1813NT	req	QAT	42	4	No	No	0	2400	2.2	2.4 / 2.4	50G	10G
D-1846	req	Comp.	55	10	No	No	0	2933	2.0	2.6 / 3.1	0G	OFF
D-1739	req	Comp.	83	8	No	No	0	2933	3.0	3.5 / 3.5	0G	OFF
D-1736	req	Comp.	55	8	No	No	0	2933	2.3	2.8 / 3.4	0G	OFF
D-1834	req	Comp.	42	8	No	No	0	2667	1.8	2.4 / 2.9	0G	OFF
D-1726	req	Comp.	70	6	No	No	0	2933	2.9	3.4 / 3.5	0G	OFF
D-1722NE	req	Comp.	36	6	No	Yes	-40	2400	1.7	2.1 / 2.7	0G	OFF
D-1714	req	Comp.	38	4	No	No	0	2667	2.3	2.8 / 3.4	0G	OFF
D1702	req	Comp.	25	2	No	No	0	2400	1.6	1.7 / 1.7	0G	OFF

DTR (Dynamic Temperature Range) limits apply.The behavior is described in Intel document #595914

3.3. COM Express Compliance

The COMe-bID7 can be offered in two different versions regarding the compliance to the COM Express COM.0 specification Rev 3.0 or Rev 3.1.

The main different between both is the support of PCIe Gen 4.0 and the pin definition for the 10G LAN interfaces

Table 5: COM Express Compliance

	PCI Express	10G Ethernet
COM.0 Rev 3.1 (default)	PCIe Gen 4.0 on COMe PCIe #16-31 2nd PCIe Clk to carrier	CEI-mode (see chapter 3.10)
COM.0 Rev 3.0 (on request)	PCIe Gen 3.0 on COMe PCIe #16-31	Legacy mode (see chapter 3.10)

3.3.1. COM.0 Rev 3.1: default configuration:

10G LAN - CEI (Common Electrical Interface) mode

This mode is used on COMe-bID7 modules for carriers/backplanes designed according to the COM Express specification COM.0 Rev 3.1 and newer. In comparison to the legacy mode the CEI mode consists of a fewer set of signals between module and carrier/backplane. Additional components required for a particular Ethernet mode – such as LED controller, etc.. - are populated on the carrier/backplane

PCI Express Gen4 support

The COMe PCIe #0-15 from the SOC-PCH hosts PCIe Gen3 root devices and provides the necessary clock.

The COMe PCIe #16-31 from the CPU hosts PCIe Gen4 root devices, but needs a high accuracy external clock source. The additional clock source provides the reference clock to the CPU and also to the Carrier board PCIe Gen4 target, over the 2nd set of PCIe clock reference pins provided in COM.0 Rev 3.1.

3.3.2. COM.0 Rev 3.0: available on request (legacy mode)

10G LAN - **"legacy" mode**

For selected 10GbE modes the required additional components are directly populated on the COMe-bID7 module. The legacy mode enables those components on the module, which allow using the COMe-bID7 module on carriers/backplanes designed according to the COM Express specification COM.0 Rev 3.0.

PCI Express Gen3 support

There is a single 100 MHz PCI Express reference clock delivered over the COM Express connector.

3.4. Memory

Up to 4x SODIMM Socket DDR4 non-ECC/ECC, height: 4+8mm

2x SODIMM sockets on top side – max. DDR4-2933 MT/s (depends on the processor SKU)

Optional additional 2x SODIMM sockets on the bottom side (this is out of the PICMG specification) – max. DDR4-2666 MT/s (depends on the processor SKU)

> Second SO-DIMM (bottom side of module) exceeds the maximum height for COM Express modules defined by the PICMG specification between carrier and module, even with an 8mm connector stack-up. Special care has to be taken for the Carrier Board design – a cut-out area is recommended.

Table 6: Memory Features

Socket	Default: 2x DDR4 SO-DIMM On request: 4x DDR4 SODIMM
Memory Type	DDR4, up to 2933 MT/s, up to 32 GB per socket
Memory Module Capacity	8, 16 and 32 GB

3.5. PCI Express 4.0

The SoC CPU supports 16x PCIe Gen 4.0 lanes used to support COMe PCIe #16-31 with one Root Complex (RPC) and four Root Ports (RP) max.

Table 7: SoC – PCI Express Gen. 4.0

Module Function	SoC PCIE Function	Lane Configuration				
		x1	x2	x4	x8	x16
COMe PCIE #16	PCIE 4.0 #0	-	-	x	x	x
COMe PCIE #17	PCIE 4.0 #1	-				
COMe PCIE #18	PCIE 4.0 #2	-	-			
COMe PCIE #19	PCIE 4.0 #3	-				
COMe PCIE #20	PCIE 4.0 #4	-	-	x		
COMe PCIE #21	PCIE 4.0 #5	-				
COMe PCIE #22	PCIE 4.0 #6	-	-			
COMe PCIE #23	PCIE 4.0 #7	-				
COMe PCIE #24	PCIE 4.0 #8	-	-	x	x	
COMe PCIE #25	PCIE 4.0 #9	-				
COMe PCIE #26	PCIE 4.0 #10	-	-			
COMe PCIE #27	PCIE 4.0 #11	-				
COMe PCIE #28	PCIE 4.0 #12	-	-	x		
COMe PCIE #29	PCIE 4.0 #13	-				
COMe PCIE #30	PCIE 4.0 #14	-	-			
COMe PCIE #31	PCIE 4.0 #15	-				

3.6. HSIO Usage

The SoC PCH supports 24x HSIO lanes #0-23 (HSIO) which can be configured as PCIe Gen 3.0 lanes with up to 3 RPC, 4 RP per RPC (12 RPs max). The HSIO PCIE lanes are partly multiplexed with USB3.0 and SATA.

The HSIO lanes #0 -#15 are used as PCIe Gen 3.0 to support COMe PCIe #0 -15.

The HSIO lane #16 is used as PCIe Gen 3.0 for the onboard 1 /2.5 GbE Controller Intel i225.

The HSIO lane #18 is used as PCIe Gen 3.0 for an optional onboard NVMe SSD.

Alternatively the HSIO lanes #16, #18 and #22 can be used (by BOM option) to enable PCIe x1 lanes on COMe PCIe #0, #3 and #5.

Table 8: SoC – HSIO Usage: PCI Express Gen 3.0, SATA, USB, onboard I/O

Module Function	SoC HSIO Port	BOM Option	Lane Configuration				Comment
			x1	x2	x4	x8	
COMe PCIE #0	HSIO #0		x	x	x	x	
COMe PCIE #1	HSIO #1	HSIO #18	(x)				Feature on request: PCIe lane x1 [1]
COMe PCIE #2	HSIO #2		x	x			
COMe PCIE #3	HSIO #3	HSIO #22	(x)				Feature on request: PCIe lane x1 [1]
COMe PCIE #4	HSIO #4		x	x	x		
COMe PCIE #5	HSIO #5	HSIO #16	(x)				Feature on request: PCIe lane x1 [1]
COMe PCIE #6	HSIO #6		x	x			
COMe PCIE #7	HSIO #7		-				
COMe PCIE #8	HSIO #8		x	x	x	x	
COMe PCIE #9	HSIO #9		-				
COMe PCIE #10	HSIO #10		x	x			
COMe PCIE #11	HSIO #11		-				
COMe PCIE #12	HSIO #12		x	x	x		
COMe PCIE #13	HSIO #13		-				
COMe PCIE #14	HSIO #14		x	x			
COMe PCIE #15	HSIO #15		-				
Onboard GbE0 1/2.5GbE (default)	HSIO #16	No GbE0	x				
COMe SATA #1	HSIO #17						
Onboard NVMe option (default)	HSIO #18	No NVMe option	x				
COMe SATA #0	HSIO #19						
COMe USB3 #0	HSIO #20						
COMe USB3 #1	HSIO #21						
COMe USB3 #2	HSIO #23						
COMe USB3 #3	HSIO #22	No USB3 #3					

[1] BOM options can be offered on request to allow PCIe x1 usage for COMe Lane PCIE0-PCIE5.

The following table lists the standard supported PCI Express lane configurations defined by the BIOS:

Table 9: BIOS versions

COMe Lane	Lane Configuration			
	default	var1	var2	var3
COMe PCIE #0	x4	x4	x8	x2
COMe PCIE #1				
COMe PCIE #2				x2
COMe PCIE #3				
COMe PCIE #4	x4	x4		x2
COMe PCIE #5				
COMe PCIE #6				x2
COMe PCIE #7				
COMe PCIE #8	x8	x4	x8	x4
COMe PCIE #9				
COMe PCIE #10				
COMe PCIE #11				
COMe PCIE #12		x4		x4
COMe PCIE #13				
COMe PCIE #14				
COMe PCIE #15				
COMe PCIE #16 - 31	x16	x16	x16	x16

NOTICE

Please contact Kontron Support for other BIOS configurations.

3.7. USB

USB 3.x ports are backwards compatible with the USB 2.0 specification. The COMe-bID7 allows a maximum of four USB 3.1 Gen 1 ports including four USB 2.0 ports.

Table 10: Supported USB Features

USB 3.1 Gen 1 Ports	4x USB 3.1 Gen 1

	Option: 3x USB 3.1 Gen 1 – HSIO #22 is used for COMe PCIE 3.0 lane #3 instead of USB3 #3
USB 2.0 Ports	4x USB 2.0
USB Over Current Signals	2x

See Table 8: SoC – HSIO Usage: PCI Express Gen 3.0, SATA, USB, onboard I/O.

3.8. SATA

The SATA high-speed storage interface supports two SATA Gen.3 ports with transfer rates of up to 6 Gb/s.

See Table 8: SoC – HSIO Usage: PCI Express Gen 3.0, SATA, USB, onboard I/O.

3.9. Ethernet – 1G / 2.5GBASE-T LAN

The COMe-bID7 supports one 1 GbE/2.5 GbE Base-T Ethernet interface using the Intel® i225-LM Ethernet controller for commercial temperature grades and the Intel®I225-IT for industrial temperature grades (E2).

3.10. Ethernet – 4x 10GBASE-KR

Intel® Xeon® D-1700 processor family supports up to two integrated PHY Quads with 1G/2.5G/10G/25G/40G/50G/100G rates, where with COM Express Type 7 only one PHY Quad can be used – supporting a max of 4x 10GBASE-KR ports.

Due to bandwidth limitation of the COM Express Type 7 connectors it is currently possible to use a max.of 10G rates. All interfaces of one PHY Quad must have the same configuration (same speed and same physical interface).

The COMe-bID7 can be offered in two general NIC configuration hardware options:

10G LAN CEI mode (default configuration):

This mode is intended to use on modules and carriers/backplanes designed according to COM Express specification COM.0 Rev 3.1 and newer. The CEI mode defines that all external components required for a particular Ethernet mode are located outside of the COM Express module (e.g. on COM Express carrier/backplane or an expansion card), including the CEI_ID EEPROM.

10G LAN Legacy mode (available on request):

For selected 10GbE modes the required external components are directly included on the COMe-bID7 module. The Legacy mode enables those components on the module, which allow to use the COMe-bID7 module on carriers/backplanes designed according to COM Express specification COM.0 Rev 3.0.

3.10.1. Overview of currently supported LAN Interfaces on COMe-bID7

10GBASE-KR (default configuration) – CEI

Backplane Ethernet (no external PHY required)

Typical chip to chip connection e.g. via backplane or via short direct attach cable

COMe-bID7: LAN config **LEK 7.6** – **4ports**

Evaluation Platform:

COMe Evaluation Carrier T7 (68300-0000-00-0) – Note: **COMe-bID7 must be factory-preconfigured for COM.0 R3.0 regarding PCI Express support**

COMe Evaluation Carrier T7 Gen2 A2T7 (68301-0001-00-8) and expansion card ADA-COMe-T7-G2 4X 10G DAC (68301-0000-04-4)

10G-SFI (on request) – CEI

Used for optical connection (optical SFP+ modules for multi-mode or single-mode fiber)

SFP+ direct attach (copper cable)

Extra PHY (Intel® C827/XL827) is required on carrier board

COMe-bID7: LAN config **LEK 7.0** – **4ports**

Evaluation Platform:

COMe Evaluation Carrier T7 Gen2 (68301-0001-00-8) and expansion card ADA-COMe-T7-G2 4x 10G SFP+ C827-IM1 (68301-0000-05-4)

10G-SFI native (on request) – legacy

Used for optical connection (optical SFP+ modules for multi-mode or single-mode fiber)

SFP+ direct attach (copper cable)

COMe-bID7: LAN config **LEK 1.0** – **4ports**

Evaluation Platform:

COMe Evaluation Carrier T7 (68300-0000-00-0) - **Note: COMe-bID7 must be factory-preconfigured for COM.0 R3.0 regarding PCI Express support**

or

COMe Evaluation Carrier T7 Gen2 (68301-0001-00-8) and expansion card ADA-COMe-T7-G2 4X 10G DAC (68301-0000-04-4) – no PHY

10GBASE-T (on request) – legacy

10 Gbps connection over twisted pair CAT6A cables with distances up to 100 meters

Typical RJ45 connection

Extra PHY (Intel® X557) is required on carrier board

COMe-bID7: LAN config **LEK 2.1** – **4ports**

Evaluation Platform:

COMe Evaluation Carrier T7 Gen2 (68301-0001-00-8) and expansion card ADA-COMe-T7-G2 4x 10G RJ45 (68301-0000-01-4).

NOTICE Other 10G LAN configurations are available as well on request, however at this point of time w/o a corresponding evaluation platform.

Please contact Kontron Support for further assistance.

NOTICE

Please refer to the Application Note at EMD Customer Section (Customer Section | Kontron Europe and Asia.

3.11. UART

The UART serial communications interface supports up to two serial RX/TX ports supplied by the SOC. The two serial ports are defined in the COMe specification on pins A98 (SERO_TX) and A99 (SERO_RX) for UART0, and pins A101 (SER1_TX) and A102 (SER1_RX) for UART1.

3.12. Additional Features

Table 11: General, Special Kontron and Optional Features

General Features	
4x 10G Ethernet	PICMG COM.0 R3.1 compliance – CEI-interface
4x 10G Ethernet-LEK	10GBASE-KR: LEK 7.6-4ports
PCI Express COMe #16-31	PICMG COM.0 R3.1 compliance
Fast I2C	Connected to module EEPROM, carrier EEPROM and RTC clock
SPI	SPI external boot
LPC	Used for external LPC on carrier board
RTC	Supported
SM Bus	Supported

Special Kontron Features	
Embedded API	KEAPI 3 for all Supported OS KEAPI packages are included in reference image
TPM 2.0	1x TPM 2.0 (hardware)
GPIO	Start-up level configurable, GPI interrupt capable
Watchdog Support	Dual staged

Optional Features (on request)	
4x 10G Ethernet	PICMG COM.0 R3.0 compliance
4x 10G Ethernet-LEK	Configurations for: SFI native: LEK 1.0-4ports (COM.0 R3.0) 10GBASE-T: LEK 2.1-4ports (COM.0 R3.0) CEI: LEK 7.0-4ports (COM.0 R3.1)
PCI Express COMe #16-31	PICMG COM.0 R3.0 compliance
PCI Express COMe #0-7	Enable PCIe x1 lanes on COMe PCIe #1, #3, #5
NVMe SSD	Up to 1 TByte NVMe PCIe SSD NAND Flash
2nd SPI Flash	On-module fail-safe 2nd SPI flash implemented for additional safety
SODIMM sockets	4x SODIMM sockets (2x on top side + 2x on bottom side)
SODIMMs	Non-ECC SODIMMs
CPU	other CPUs than offered as standard versions
BIOS	custom BIOS configurations

3.13. Evaluation platforms for COMe-bID7 – Compatibility Matrix

Please see below the possible combinations regarding the COMe-bID7 configuration and the matching evaluation platform

COMe-bID7				Evaluation Platform		
PCIe Implementation	LAN Implementation	LAN Config and related LEK file		Carrier - PCIe Gen3 only	Adapter / Expansion	PHY
COM.0 R3.0	COM.0 R3.0 or COM.0 R3.1	4x 10GBASE-KR	7.6	COMe Eval Carrier T7 68300-0000-00-0	none	none
				COMe Eval Carrier2 T7-G2 68301-0000-00-8 (or -5)	ADA-COMe-T7-G2 4X 10G DAC - DEV-TOOL 68301-0000-04-4	none
COM.0 R3.0	COM.0 R3.0	4x 10G-SFI native	1.0	COMe Eval Carrier T7 68300-0000-00-0	none	none
				COMe Eval Carrier2 T7-G2 68301-0000-00-8 (or -5)	ADA-COMe-T7-G2 4X 10G DAC - DEV-TOOL 68301-0000-04-4	none
COM.0 R3.0	COM.0 R3.0	4x 10GBASE-T	2.1	COMe Eval Carrier2 T7-G2 68301-0000-00-8 (or -5)	ADA-COMe-T7-G2 4x 10G RJ45 - DEV-TOOL 68301-0000-01-4	PHY = 2x X557-AT2
COM.0 R3.0	COM.0 R3.1	4x 10G-SFI with PHY (CEI)	7.0	COMe Eval Carrier2 T7-G2 68301-0000-00-8 (or -5)	ADA-COMe-T7-G2 4x 10G SFP+ - C827-IM1 – DEV-TOOL 68301-0000-05-4	PHY = C827-IM1
				Carrier - PCIe Gen4 support		
COM.0 R3.1 *	COM.0 R3.0 or ***COM.0 R3.1 ****	***4x 10GBASE-KR ****	***7.6 ****	COMe Eval Carrier2 T7-G2 68301-0001-00-8 (or -5)	ADA-COMe-T7-G2 4X 10G DAC - DEV-TOOL 68301-0000-04-4	none
COM.0 R3.1	COM.0 R3.0	4x 10G-SFI native	1.0	COMe Eval Carrier2 T7-G2 68301-0001-00-8 (or -5)	ADA-COMe-T7-G2 4X 10G DAC - DEV-TOOL 68301-0000-04-4	none
COM.0 R3.1	COM.0 R3.0	4x 10GBASE-T	2.1	COMe Eval Carrier2 T7-G2 68301-0001-00-8 (or -5)	ADA-COMe-T7-G2 4x 10G RJ45 - DEV-TOOL 68301-0000-01-4	PHY = 2x X557-AT2
COM.0 R3.1	COM.0 R3.1	4x 10G-SFI with PHY (CEI)	7.0	COMe Eval Carrier2 T7-G2 68301-0001-00-8 (or -5)	ADA-COMe-T7-G2 4x 10G SFP+ - C827-IM1 – DEV-TOOL 68301-0000-05-4	PHY = C827-IM1

*** COMe-bID7 default configuration**

4/ Features and Interfaces

4.1. ACPI Suspend Modes and Resume Events

The COMe-bID7 supports the S-states S0 and S5.

The following event resumes the system from S5:

- Power Button
- Wake-on-LAN

4.2. Real Time Clock (RTC)

The RTC keeps track of the current time accurately. The RTC's low power consumption enables the RTC to continue operation and keep time using a lower secondary source of power while the primary source of power is switched off or unavailable.

The COMe-bID7 supports typical RTC values of 3 V and less than 10 µA. When powered by the mains power supply on-module regulators generate the RTC voltage, to reduce RTC current draw. The RTC's battery voltage range is 2.8 V to 3.47 V.

It is not recommended to run a system without a RTC battery on the carrier board. Even if the RTC battery is not required to keep the actual time and date when main power is off, a missing RTC battery will cause other side effects such as longer boot times. Intel processor environments are generally designed to rely on RTC battery voltage.

4.3. NVMe Storage (Option)

The NVMe SSD Flash memory supports up to one TByte. The optional NVMe SSD uses HSIO #18 of the SoC.

4.4. Hardware Monitor (HWM)

The Hardware Monitor (HWM) controls the health of the system by monitoring critical aspects such as temperatures, power supply voltages and fan speed for cooling. The temperature is controlled by temperature sensors supported via the SMBus interface and directly from the CPU using Intel's® Platform Environment Control Interface (PECI) 3.0 interface. The SMART FAN™ technology controls the duty cycle of the fan output with temperature setting points. This enables flexible fan control for cooling solutions and noise sensitive solutions. For system protection, users can set threshold values for alarm signals.

4.5. Trusted Platform Module (TPM)

A Trusted Platform Module (TPM) stores RSA encryption keys specific to the host system for hardware authentication. The term TPM refers to the set of specifications applicable to TPM chips. The SPI bus connects the TPM chip to the CPU.

Each TPM chip contains an RSA key pair called the Endorsement Key (EK). The pair is maintained inside the chip and cannot be accessed by software. The Storage Root Key (SRK) is created when a user or administrator takes ownership of the system. The TPM generates the key pair based on the Endorsement Key and an owner-specified password.

A second key, called an Attestation Identity Key (AIK) protects the device against unauthorized firmware and software modification by hashing critical sections of firmware and software before they are executed. When the system attempts to connect to the network, the hashes are sent to a server that verifies that they match the expected values. If any of the hashed components have been modified since the last start, the match fails, and the system cannot gain entry to the network.

4.6. Onboard Fan Connector

The analog output voltage on this connector is generated via a discrete linear voltage regulator from the PWM signal of the HWM. It is clipped at 12 V (+/- 10 %) across the whole input range of the module to prevent fan damage at higher voltages.

The maximum supply current to the fan connected to the on-module fan connector is 350 mA if the input voltage is below 13.0 V and is further limited to 150 mA if the input voltage to the module is between 13.0 V and 20.0 V.

Table 12: Onboard Fan Connector

Pin	Signal	Description	Type
1	Fan_Tach_IN#	Fan Input voltage from COMe connector	Input
2	V_FAN	12 V ±10% (max.) across module input range	PWR
3	GND	Power GND	PWR

NOTICE

Always check the fan specification according to the limitations of the supply current and supply voltage.

4.7. Watchdog Timer (WDT) Dual Stage

The watchdog timer interrupt is a hardware or software timer implemented by the module to the carrier board if there is a fault condition in the main program; the watchdog triggers a system reset or other corrective actions after a specific time, with the aim to bring the system back from a non-responsive to normal state.

The COMe-bID7 supports an independently programmable watchdog that works with two stages that can be used stage by stage.

Table 13: Dual Staged Watchdog Timer- Time-Out Events

0000b	No action	Stage is off and will be skipped
0001b	Reset	Restarts the module and starts a new POST and operating system
0101b	Delay -> No action	Might be necessary when an operating system must be started and the time for the first trigger pulse must be extended. Only available in the first stage!
1000b	WDT Only	Triggers WDT pin on the carrier board connector (COM Express® pin B27) only
1001b	Reset + WDT	
1101b	DELAY + WDT -> No action	

4.8. Watchdog Timer Signal

The watchdog interrupt (WDT) on COM Express® pin B27 on COM Express® connector indicates a Watchdog time-out event has not been triggered within a set time. The WDT signal is configurable to any of the two stages. After reset, the signal is automatically de-asserted. If de-assertion is necessary during runtime, contact Kontron Support for further help.

4.9. Hyper-Threading

Hyper-Threading (officially termed Hyper Threading Technology or HTT) is an Intel®-proprietary technology used to improve parallelization of computations performed on PCs. Hyper-Threading works by duplicating certain sections of the processor – those that store the architectural state but not duplicating the main execution resources. This allows a Hyper-Threading equipped processor to pretend to be two "logical" processors to the host operating system, allowing the operating system to schedule two threads or processes simultaneously. Hyper-Threading Technology always depends on the Operating System.

4.10. Fast I2C

The internal I2C bus transfers data between components on the same module and the external I2C bus transfers data between I2C devices connected on the bus. The Fast I2C bus transfers data with rates up to 400 kHz.
To change the I2C bus speed, in the BIOS setup menu select:

Advanced>Miscellaneous>I2C Speed> 400 kHz to 1 kHz

The default speed is 200 kHz.

The following table specifies the devices connected the accessible I2C bus including the I2C address. The I2C bus is available at the COM Express® connector pin B33, I2C_CK and pin B34, I2C_DAT.

Table 14: I2C Bus Port Address

8-bit Address	7-bit Address	Used For	Available
A0h	50h	Module embedded EEPROM (Eeep)	Yes
AEh	57h	Carrier board EEPROM	Optional

4.11. LPC

The Low Pin Count (LPC) interface is pin shared with eSPI, where the LPC interface is the default connection from the embedded controller to the COMe connector.

The Low Pin Count (LPC) Interface signals are connected to the LPC Bus located in the Soc. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller that typically combines legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® specification. The COM Express® Design Guide maintained by PICMG provides implementation information or refer to the official PICMG documentation for more information.The LPC bus does not support DMA (Direct Memory Access). When more than one device is used on LPC, a zero delay clock buffer is required. This leads to limitations for ISA bus and SIO (standard I/O(s) like floppy or LPT interfaces) implementation. The COMe-bID7 LPC clock buffer allows for the connection of three LPC devices

4.12. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) bus is a synchronous serial data link where devices communicate in master/slave mode and the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

4.12.1. SPI Boot

The COMe-bID7 supports on-module and on-carrier boot from an SPI Flash.

The pins A34 (BIOS_DIS0#) and B88 (BIOS_DIS1#) configure the SPI Flash to be used, see Table 15.

Table 15: SPI Boot Pin Configuration

BIOS_DIS0#	BIOS_DIS1#	Boot Bus	Function
Open	Open	SPI	Boot on-module SPI
Open	GND	SPI	Boot on-carrier SPI

Table 16: Supported SPI Boot Flash

Size	Manufacturer	Part Number	Package Type	Manufact. ID
32 MByte	Winbond	W25Q256JVEIQ	WSON-8 8x6 mm	EFh

4.12.2. SPI Flash Update

1. On-board SPI Flash

Initially, the EFI Shell is booted with an USB key containing the binary used to flash the on-module SPI Flash chip.

The command line is:
AfuEfix64 \ EtaAfuOemEfi64.efi BID7Rxxx.bin /p /b /n /k /me /x

i

It intentionally does not flash the 10GbE region to avoid destroying 10GbE MAC addresses when only Bios update is required.

See further information in the BIOS package itself available on Kontron's Customer Section.

2. External SPI Flash

To program the external SPI Flash on the carrier board with the BIOS binary, use an external programmer.

When booting from the external SPI Flash on the carrier board if the COM Express® module is exchanged for another module of the same type, the Intel® Management Engine (ME) will fail during the next start. The Management Engine (ME) binds itself to every module it has previously flashed which in the case of an external SPI Flash is the module present when flashed.

i

To avoid this issue, after changing the COM Express® module for another module, conduct a complete flash from the external SPI Flash device. If disconnecting and reconnecting the same module again, this step is not necessary.

i

Register for Kontron's Customer Section to get access to BIOS downloads and PCN service.

4.13. System Management Bus (SMB)

The System Management Bus (SMB) is a simple 2-wire bus for low-speed system management communication. The PCH controls the SMB. The module's SMB, routed to the COMe connector connects to the hardware controller and the optional NVMe.

The 8-bit SMBus address uses the LSB (bit 0) for the direction of the device.

- Bit0 = 0 defines the write address
- Bit0 = 1 defines the read address

The following table specifies the 8-bit and 7-bit SMBus write address for all devices.

Table 17: SMBus Address

8-bit Address	7-bit Address	Device	Description
0x10	0x08	SoC - reserved	
0x5C	0x2E	Hardware Monitor NCT7802Y	Do not use this address for external devices under any circumstances
0x88	0x44	SoC - reserved	
0xD4	0x6A	PCIe Clock Buffer	

4.14. GPIO

The eight GPIO pins support four inputs pins (A54 for GPI0, A63 for GPI1, A67 for GPI2 and A85 for GPI3) and four output pins (A93 for GPO0, B54 for GPO1, B57 for GPO2 and B63 for GPO3) by default. The four GPI[0-3] pins are pulled high with a pull-up resistor (e.g. 100 K ohms) and the four GPO[0-3] pins are pulled low with a pull-down resistor (e.g. 100 K ohms) on the module.

To change the default GPIO signal-state users are required to make BIOS and/or OS-driver changes, and additional hardware changes by adding external termination resistors on the carrier board to override the weak on-module pull-up resistors with a lower resistance pull-down (e.g. 10 K ohms), or pull-down resistors with a lower resistance pull-up (e.g. 10 K ohms).

4.15. NS-CI

The COMe-bID7 supports the NC-SI (Network Controller Sideband Interface) physical interface. The NC-SI signals from the D-1700 SOC are routed to the COMe connector.

5/ Accessories

5.1. Product Specific Accessories

Table 18: Product Specific Accessories List

Product Number	Carrier	Description
Standard		
68300-0000-00-0	COMe Eval Carrier T7	COM Express® Eval Carrier Type 7
68301-0001-00-8	COMe Eval Carrier T7 G2-8 R3.1	COM Express® Eval Carrier Type 7 Gen2, 8 mm stack-up, according COM.0 Rev 3.1
68301-0000-00-8	COMe Eval Carrier T7 G2-8 R3.0	COM Express® Eval Carrier Type 7 Gen2, 8 mm stack-up, according COM.0 Rev 3.0
Available on request		
68301-0001-00-5	COMe Eval Carrier T7 G2-5 R3.1	COM Express® Eval Carrier Type 7 Gen2, 5 mm stack-up, according COM.0 Rev 3.1
68301-0000-00-5	COMe Eval Carrier T7 G2-5 R3.0	COM Express® Eval Carrier Type 7 Gen2, 5 mm stack-up, according COM.0 Rev 3.0

Product Number	**AdapterCards to be used with COMe Eval Carrier T7 G2**	**Description**
68301-0000-01-4	ADA-COMe-T7-G2 4x 10G RJ45 - DEV-TOOL	4x RJ45: 10GBASE-KR-to-10GBASE-T via 2x Intel PHY X557-AT2
68301-0000-04-4	ADA-COMe-T7-G2 4X10G DAC - DEV-TOOL	4x DAC: 10GBASE-KR signals directly routed from COMe connector to SFP+ cages
68301-0000-05-4	ADA-COMe-T7-G2 4x10G SFP+ - C827-IM1 – DEV-TOOL	4x SFP+: 10GBASE-KR-to-SFI via Intel PHY C827-IM1

Table 19: Cooler and Heatspreader

Product Number	Product	Description
68009-0000-99-0	HSP COMe-bID7 (E2) threaded mounting holes	Heatspreader for COMe-bID7 (E2), with Cu-core, threaded mounting holes
68009-0000-99-1	HSP COMe-bID7 (E2) through holes	Heatspreader for COMe-bID7 (E2), with Cu-core, through holes
38025-0000-99-0C05	HSK COMe-basic active (w/o HSP)	Active Cooler for COMe-bID7 to be mounted on HSP
38025-0000-99-0C06	HSK COMe-basic passive (w/o HSP)	Passive Cooler for COMe-bID7 to be mounted on HSP

5.2. General Accessories

Table 20: General Accessories List

Product Number	Mounting	Description
38017-0000-00-5	COMe Mount KIT 5mm 1set	Mounting Kit for 1 module including screws for 5mm connectors
38017-0000-00-0	COMe Mount KIT 8mm 1set	Mounting Kit for 1 module including screws for 8mm connectors
Product Number	Cables	Description
96079-0000-00-0	KAB-HSP 200mm	Cable adapter to connect Fan to module (COMe basic/compact)
96079-0000-00-2	KAB-HSP 40mm	Cable adapter to connect Fan to module (COMe basic/compact)

Table 21: Memory Modules

Part Number	Memory (ECC)	Description
97030-0832-BID7	DDR4-3200 SODIMM 8 GB_BID7	DDR4-3200, 8 GB, 260P, 1600 MHz, PC4-3200 SODIMM, ECC
97030-1632-BID7	DDR4-3200 SODIMM 16 GB_BID7	DDR4-3200, 16 GB, 260P, 1600 MHz, PC4-3200 SODIMM, ECC
97030-3232-BID7	DDR4-3200 SODIMM 32 GB_BID7	DDR4-3200, 32 GB, 260P, 1600 MHz, PC4-3200 SODIMM ECC
97031-0832-BID7	DDR4-3200 SODIMM 8 GB E2_BID7	DDR4-3200, 8 GB, 260P, 1600 MHz, PC4-3200 SODIMM, ECC, industrial temperature
97031-1632-BID7	DDR4-3200 SODIMM 16 GB E2_BID7	DDR4-3200, 16 GB, 260P, 1600 MHz, PC4-3200 SODIMM, ECC, industrial temperature
97031-3232-BID7	DDR4-3200 SODIMM 32 GB E2_BID7	DDR4-3200, 32 GB, 260P, 1600 MHz, PC4-3200 SODIMM, ECC, industrial temperature

Non-ECC SODIMMs are available on request.

6/ Electrical Specification

6.1. Supply Voltage

Table 22 provides information regarding the supply voltage specified at the COM Express® connector.

Table 22: COM Express® Connector Electrical Specifications

	Commercial Grade	Industrial Grade
VCC	8.5 V – 20 V	12 V DC +/- 5%
Standby	5V DC +/- 5% (5 VSB is not mandatory for operation)	5 V DC +/- 5%
RTC	2.8 V - 3.47 V	2.8 V - 3.47 V

5 V Standby voltage is not mandatory for operation.

6.2. Power Supply Rise Time

The input voltages should rise from ≤10% of nominal to within the regulation ranges within 0.1 ms to 20 ms.

There must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of its final set-point following the ATX specification.

6.3. Supply Voltage Ripple

Maximum 100 mV peak to peak 0 – 20 MHz.

6.4. Power Consumption

The COMe-bID7 supports D-1700 processor SKUs up to 90 W TDP.

For Information on Detailed Power Consumption measurements in all states and benchmarks for CPU, Graphics and Memory performance, refer to the Application Note at EMD Customer Section (Customer Section | Kontron Europe and Asia).

6.5. ATX Mode

By connecting an ATX power supply with VCC and 5VSB, PWR_OK is set to low level and VCC is off. Press the Power Button to enable the ATX PSU setting PWR_OK to high level and powering on VCC. The ATX PSU is controlled by the PS_ON# signal which is generated by SUS_S3# through inversion.

In ATX Mode VCC can be 8.5 V – 20 V for commercial grade modules and 12 V DC +/- 5% for industrial grade modules.

Table 23: ATX Mode

State	PWRBTN#	PWR_OK	V5_StdBy	PS_ON#	VCC
G3	x	x	0V	x	0V
S5	high	low	5V	high	0V
S5 → S0	PWRBTN Event	low → high	5V	high → low	0 V→ VCC
S0	high	high	5V	low	VCC

6.6. Single Supply Mode

In single supply mode, without 5V standby the module will start automatically when VCC power is connected and Power Good input is open or at high level (internal PU to 3.3V).

VCC can be 8.5 V – 20 V for commercial grade modules and 12 V DC +/- 5% for industrial grade modules.

To power on the module from S5 state press the power button or reconnect VCC. Suspend/Standby States are not supported in Single Supply Mode.

Table 24: Single Supply Mode

State	PWRBTN#	PWR_OK	V5_StdBy	VCC
G3	0	0	0	0
G3 → S0	high	open / high	OPEN	connecting VCC
S5	high	open / high	OPEN	VCC
S5 → S0	PWRBTN Event	open / high	OPEN	reconnect VCC

i

All ground pins have to be tied to the ground plane of the carrier board.

NOTICE

If any of the supply voltages drops below the allowed operating level longer than the specified hold-up time, all the supply voltages should be shut down and left OFF for a time long enough to allow the internal board voltages to discharge sufficiently.
If the OFF time is not observed, parts of the board or attached peripherals may work incorrectly or even suffer a reduction of MTBF.
The minimum OFF time depends on the implemented PSU model and other electrical factors and needs to be measured individually for each case.

7/ Power Control

7.1. Power Supply

The COMe-bID7 supports a power input from 8.5 V to 20 V in the commercial grade version, but 12 V DC +/- 5% in the industrial version. The supply voltage is applied through the VCC pins (VCC) of the module connector.

Optionally 5 V +/- 5% can be applied to the V_5V_STBY pins and allows support for wake-up suspend-to-disk and soft-off state when the VCC power is removed.

Suspend-to-RAM (S3) and Hibernate (S4) is not supported by the Xeon D-1700 product family.

7.2. Power Supply Control Settings

The power supply control settings are set in the BIOS and enable the module to shut down, rest and wake from standby properly.

Table 25: Power Supply Control Settings

Power Button (PWRBTN#)	Pin B12	To start the module using the power button, the PWRBTN# signal must be at least 50 ms (50 ms ≤ t < 4 s, typical 400 ms) at low level (Power Button Event). Pressing the power button for at least four seconds turns off power to the module (Power Button Override).
Power Good (PWR_OK)	Pin B24	PWR_OK is internally pulled up to 3.3 V and must be at the high level to power on the module. This can be driven low to hold the module from powering up as long as needed. The carrier needs to release the signal when ready. Low level prevents the module from entering the S0 state (Wake up event). A falling edge during S0 (Wake up event) causes a direct switch to S5 (Power Failure).
Reset Button (SYS_RESET#)	Pin B49	When the SYS_RESET# pin is detected active (falling edge triggered), it allows the processor to perform a "graceful" reset, by waiting up to 25 ms for the SMBus to go idle before forcing a reset, even though activity is still occurring. Once the reset is asserted, it remains asserted for 5 ms to 6 ms regardless of whether the SYS_RESET# input remains asserted or not.
SM-Bus Alert (SMB_ALERT#)	Pin B15	With an external battery manager present and SMB_ALERT #connected, the module always powers on even if the BIOS switch "After Power Fail" is set to "Stay Off".
Battery low (BATLOW#)	Pin A27	BATLOW# can be used as a power fail indication a Type 7 system where assertion prevents wake from S3-S5 states.

8/ Standards and Certification

The COMe-bID7 complies with the listed European Council directives or the latest status thereof:

- European Council directive relating to Electromagnetic Compatibility (2014/30/EU)
- General Product safety Directive (2001/95/EC)
- Low Voltage directive (2014/35/EU)

The following table provides information regarding standards that are elements of the CE declaration and additional standard compliancy information. For more information, contact Kontron Support.

Table 26: Standards and Certification Compliance

Standard		Definition
EMC	Emission	EN 55032:2015 + A11:2020 Electromagnetic compatibility of multimedia equipment - Emission Requirements
	Immunity	EN IEC 61000-6-2:2019 Electromagnetic compatibility (EMC) – Part 6-2: Generic standards – Immunity standard for industrial environment
CE		Complies with the European Council Directive on the approximation of the laws of the member states relating to Electromagnetic Compatibility 2014/30/EU, General Product Safety Directive 2001/95/EC, Low Voltage Directive 2014/35/EU and Restriction of Hazardous Substances in Electrical and Electronic Equipment, RoHS Directive 2011/65/EU + 2015/863/EU + 2017/2102/EU or the latest status thereof. EN 62368-1:2014/AC:2015: Audio/video , information and communication technology equipment Part 1: Safety requirements EN IEC 62368-1:2020/A11:2020: Audio/video, information and communication technology equipment Part 1: Safety requirements EN 55032:2015/A11:2020: Electromagnetic compatibility (EMC) of multimed ia equipment Emission Requirements EN 61000-6-2:2005 +Cor.:2005: Electromagnetic compatibility (EMC) - Part 6-2: Generic standards Immunity for industrial environments+ CENELEC Cor.:2005 EN IEC 61000-6-2 :2019: Electromagnetic compatibility (EMC) - Part 6-2: Generic standards Immunity for industrial environments
UK Declaration of Conformity		BS EN 62368-1:2014/AC:2015: Audio/video, information and communication technology equipment Part 1: Safety requirements BS EN IEC 62368-1:2020/A11:2020: Audio/video, information and communication technology equipment Part 1: Safety requirements (IEC 62368-1:2018) BS EN 55032:2015/A11:2020: Electromagnetic compatibility of multimedia equipment - Emission Requirements BS EN 61000-6-2:2005/AC:2005: Electromagnetic compatibility (EMC) - Part 6-2: Generic standards - Immunity for industrial environments+CENELEC-Cor.:2005 BS EN IEC 61000-6-2:2019: Electromagnetic compatibility (EMC). Part 6-2:Generic Standards - Immunity for industrial environments
UL		CSA C22.2 NO. 62368-1, 3rd Ed.
Shock		DIN EN 60068-2-27: February 2010 Non-operating shock – (half-sinusoidal, 11 ms, 15 g)
Vibration		DIN EN 60068-2-6: October 2008 Non-operating vibration – (sinusoidal, 10 Hz – 2000 Hz, +/- 0.15 mm, 2 g)
RoHS		Directive 2011/65/EU Restriction of Hazardous substance in electrical and Electronic Equipment (RoHS)
WEEE		Directive 2012/19/EU Waste Electrical and Electronic Equipment (WEEE)

Standard	Definition
REACH	Regulation (EC) No. 1907/2006 Registration, Evaluation, Authorization and Restriction of Chemicals (REACH)

8.1. MTBF

The MTBF (Mean Time Before Failure) value was calculated using a combination of the manufacturer's test data, (if available) and the Telcordia (Bellcore) issue 2, calculation for the remaining parts.

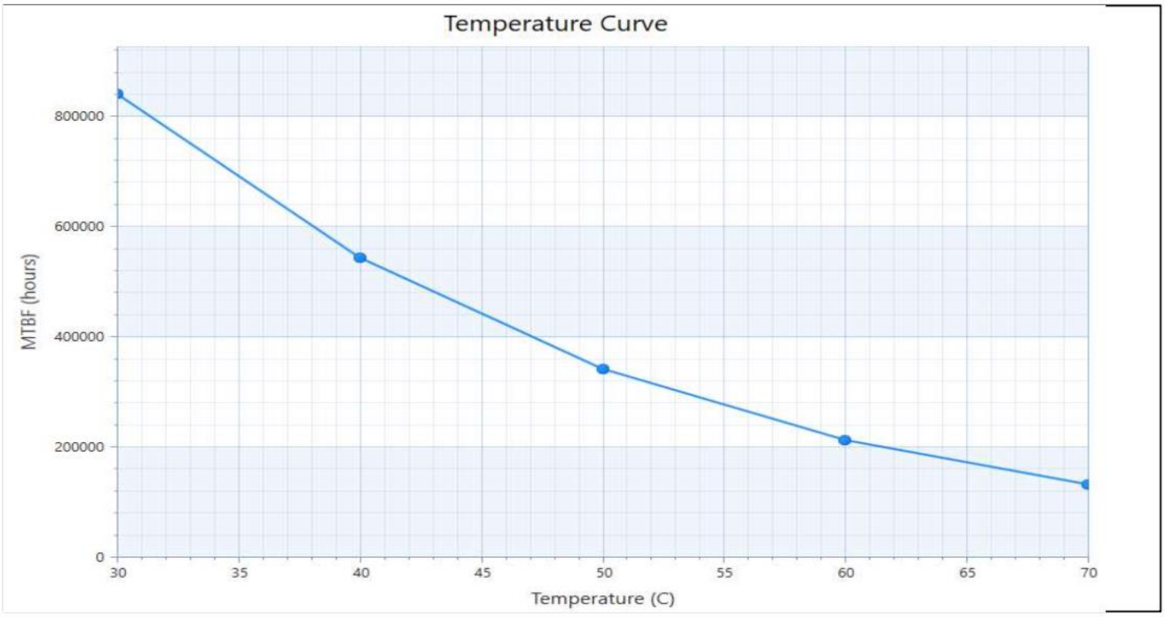
The Telcordia calculation used is "Method 1 Case 3" in a ground benign, controlled environment. This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned-in. Other environmental stresses (such as extreme altitude, vibration, salt-water exposure) lower the MTBF value.

The MTBF estimated value above assumes no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for and needs to be considered separately. Battery life depends on both temperature and operating conditions. When the module is connected to external power, the only battery drain is from leakage paths.

Figure 4 shows the MTBF de-rating value for the module variant when used in an office or telecommunications environment.

Figure 4: MTBF De-rating Values (Reliability report: COMe-bID7 E2 D-1747NTE EV)

»System MTBF(hours) = 544569 @ 40°C

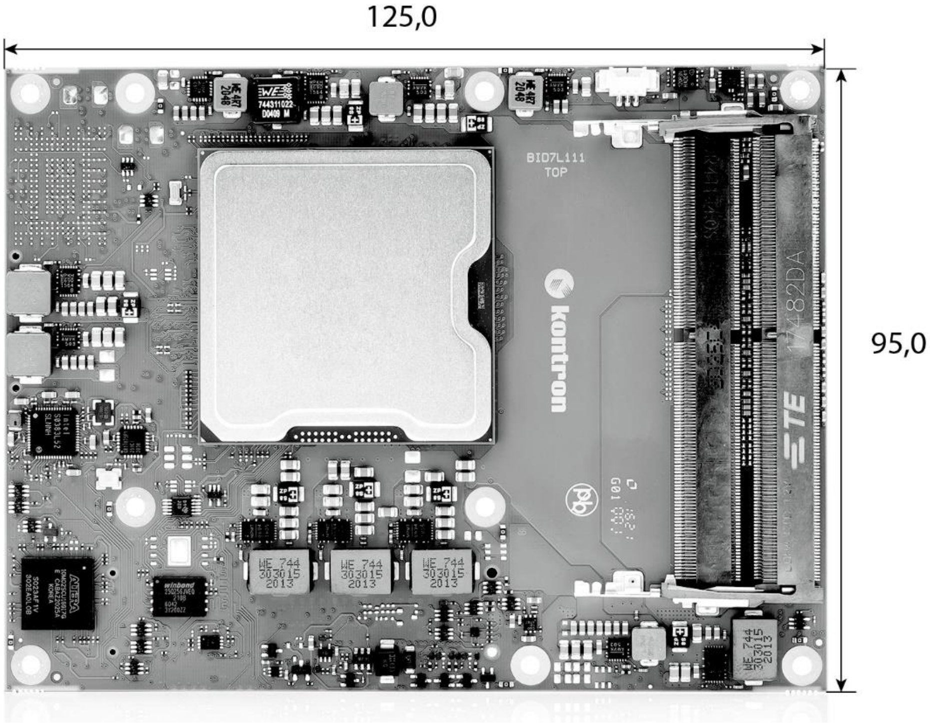


9/ Mechanical Specification

9.1. Dimensions

The dimensions of the module are 95.0 mm x 125.0 mm.

Figure 5: Module Dimensions



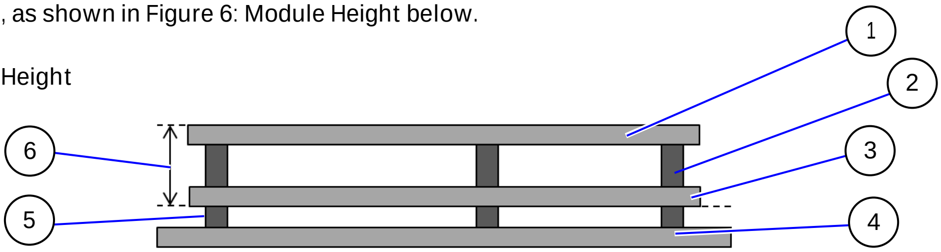
CAD drawings are available at EMD Customer Section.

9.1.1. Height

The height of the module depends on the height of the implemented cooling solution. The height of the cooling solution is not specified in the COM Express® specification.

The COM Express® specification defines a module height of approximately 13 mm from module PCB bottom to heatspreader top, as shown in Figure 6: Module Height below.

Figure 6: Module Height



1. Heatspreader
2. Heatspreaader standoff(s)
3. Module PCB
4. Carrier Board PCB
5. Connector standoff(s) 5 mm or 8 mm
6. 13 mm +/- 0.65 mm

9.1.2. Module Height with Four SODIMM Memory Sockets

The overall height of the module and carrier board depends on whether the COMe-bID7 is implemented with:

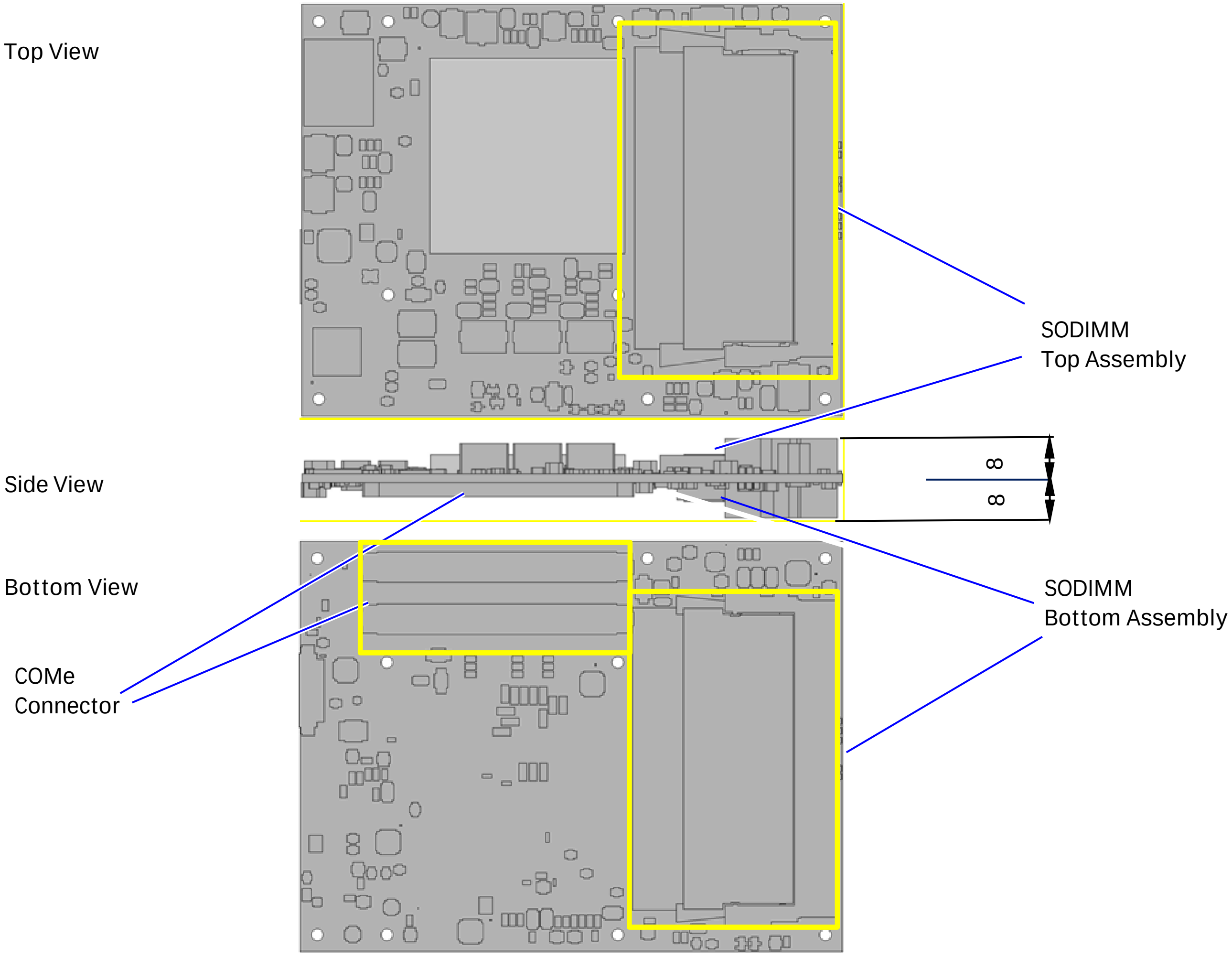
- two SODIMMs both located on module's top side (standard variant)
- four SODIMMs with two located on module's top side and bottom side

The COMe-bDV7 variant with four SODIMM memory is outside the basis COM Express® PICMG COM.0 Rev 3.0 Type 7 module form factor and requires the carrier board to be designed to support an 8 mm high COMe connector. To calculate the total height of the module and carrier take both the top side height and the bottom side height into consideration.

The 4x SODIMM variant has SODIMM sockets assembled on the bottom side of the module and requires a carrier board with 8 mm high COMe connectors and a component free area on the carrier board below the module SODIMM sockets.

The following figure shows the module board with the optional variant SODIMMs assembled on the top side and the bottom side of the board.

Figure 7: Module Top and Bottom SODIMM Assembly (Option)



9.2. Thermal Management, Heatspreader and Cooling Solutions

A heatspreader plate assembly is available from Kontron for the COMe-bID7. The heatspreader plate on top of this assembly is NOT a heat sink. It works as a COM Express®-standard thermal interface to use with a heat sink or external cooling devices.

External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature on any spot of the heatspreader's surface according the module specifications:

60°C for commercial grade modules

85°C for industrial temperature grade modules (E2/XT)

You can use many thermal-management solutions with the heatspreader plates, including active and passive approaches.

The optimum cooling solution varies, depending on the COM Express® application and environmental conditions. Active or passive cooling solutions provided from Kontron for the COMe-bID7 are usually designed to cover the power and thermal dissipation for a commercial grade temperature range used in a housing with proper air flow.

HOT Surface!
Do NOT touch! Allow to cool before servicing.

9.2.1. Heatspreader Dimensions

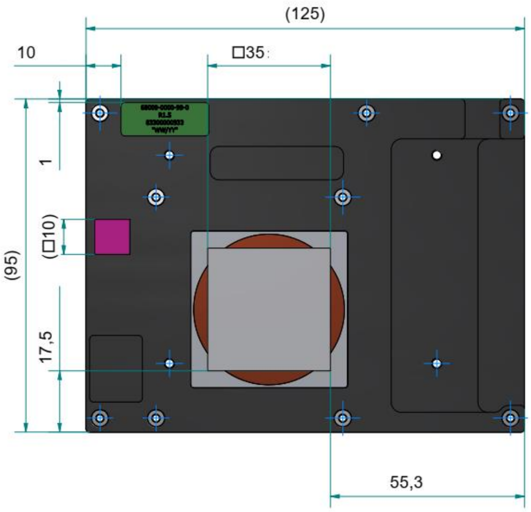
The COMe-bID7 heatspreaders are built from aluminum with a copper core. The heatspreaders have threads or through holes for mounting and are black anodized. The devices are delivered single packed.

NOTICE The heatspreaders 68009-0000-99-0 and 68009-0000-99-1 can be used with Kontron's active and passive cooling solutions 38025-0000-99-0C05 and 38025-0000-99-0C06.

9.2.1.1. Heatspreader 68009-0000-99-0 with Threads

Figure 8: Heatspreader 68009-0000-99-0 Dimensions

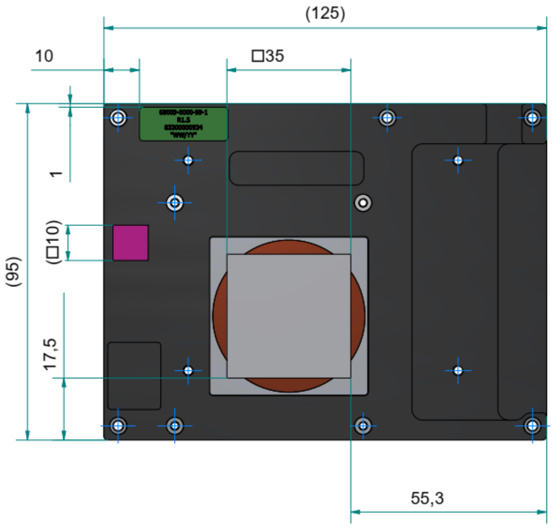
*All dimensions shown in mm.



9.2.1.2. Heatspreader 68009-0000-99-1 with Through Holes

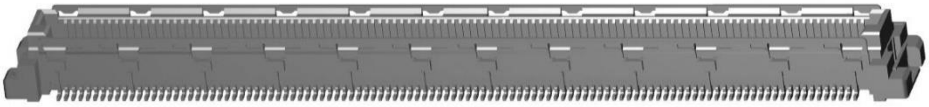
Figure 9: Heatspreader 68009-0000-99-1 Dimensions

*All dimensions shown in mm.



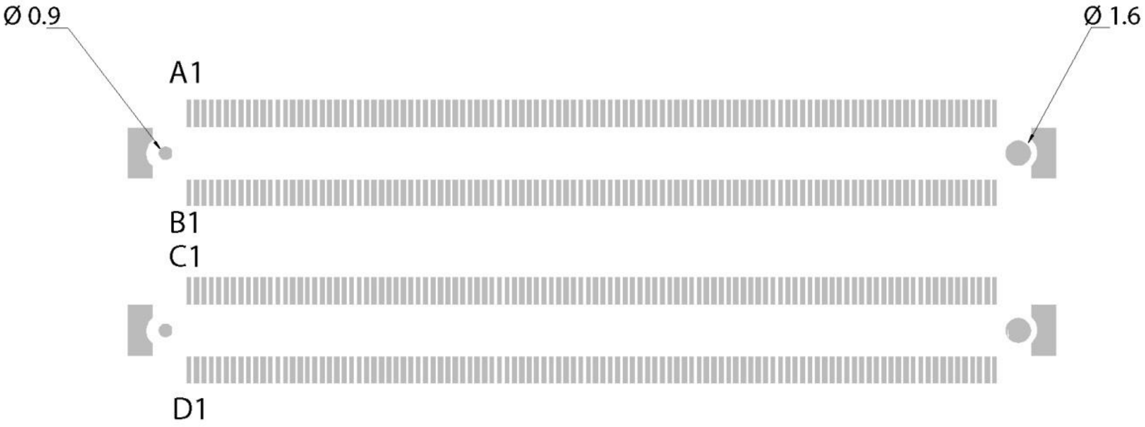
10 / COMe Connector Pin-out List

Figure 10: COMe Connector with 220 pins



This table lists the pins and signals according to the PICMG specification COM.0 Rev 3.1 and Rev 3.0 Type 7 standard.

Figure 11: COMe Connector Pinout



NOTICE

To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfills the fire-protection requirements of IEC/EN62368

Table 27: Pin-out List A

Grey background for pins different between COM.0 R.0 and R3.1

Pin	Signal	Description	Type	Termination / Comment
A1	GND	Power Ground	PWR GND	-
A2	GBE0_MDI3-	Ethernet Media Dependent Interface 3 -	DP-I/O	-
A3	GBE0_MDI3+	Ethernet Media Dependent Interface 3 +	DP-I/O	-
A4	R3.0: GBE0_LINK100# R3.1: GBE0_LINK_MID#	Ethernet Speed LED	OD	-
A5	R3.0: GBE0_LINK1000# R3.1: GBE0_LINK_MAX#	Ethernet Speed LED	OD	-
A6	GBE0_MDI2-	Ethernet Media Dependent Interface 2 -	DP-I/O	-
A7	GBE0_MDI2+	Ethernet Media Dependent Interface 2 +	DP-I/O	-
A8	GBE0_LINK#	LAN Link LED	OD	-
A9	GBE0_MDI1-	Ethernet Media Dependent Interface 1 -	DP-I/O	-
A10	GBE0_MDI1+	Ethernet Media Dependent Interface 1 +	DP-I/O	-
A11	GND	Power Ground	PWR GND	-
A12	GBE0_MDI0-	Ethernet Media Dependent Interface 0 -	DP-I/O	-
A13	GBE0_MDI0+	Ethernet Media Dependent Interface 0 +	DP-I/O	-
A14	GBE0_CTREF	Center Tab Reference Voltage	REF	1uF capacitor to GND
A15	SUS_S3#	Suspend To RAM (or deeper) Indicator	O-3.3	-
A16	SATA0_TX+	SATA Transmit Pair 0 +	DP-O	AC Coupled on Module
A17	SATA0_TX-	SATA Transmit Pair 0 -	DP-O	AC Coupled on Module
A18	SUS_S4#	Suspend To Disk (or deeper) Indicator	O-3.3	-
A19	SATA0_RX+	SATA Receive Pair 0 +	DP-I	AC Coupled on Module
A20	SATA0_RX-	SATA Receive Pair 0 -	DP-I	AC Coupled on Module
A21	GND	Power Ground	PWR GND	-

Pin	Signal	Description	Type	Termination / Comment
A22	PCIE_TX15+	PCI Express Lane 15 Transmit +	DP-O	AC Coupled on Module
A23	PCIE_TX15-	PCI Express Lane 15 Transmit -	DP-O	AC Coupled on Module
A24	SUS_S5#	Soft Off Indicator	O-3.3	-
A25	PCIE_TX14+	PCI Express Lane 14 Transmit +	DP-O	AC Coupled on Module
A26	PCIE_TX14-	PCI Express Lane 14 Transmit -	DP-O	AC Coupled on Module
A27	BATLOW#	Battery Low	I-3.3	PU 10k 3.3V (S5)
A28	SATA_ACT#	Serial ATA activity LED	O-3.3	PU 10k 3.3V (S0)
A29	RSVD	Reserved for future use	NC	-
A30	RSVD	Reserved for future use	NC	-
A31	GND	Power Ground	PWR GND	-
A32	RSVD	Reserved for future use	NC	-
A33	RSVD	Reserved for future use	NC	-
A34	BIOS_DIS0#/ESPI_SAF S	BIOS Selection Strap 0	I-3.3	PU 10k 3.3V (S5)
A35	THRMTRIP#	Thermal Trip	O-3.3	-
A36	PCIE_TX13+	PCI Express Lane 13 Transmit +	DP-O	AC Coupled on Module
A37	PCIE_TX13-	PCI Express Lane 13 Transmit -	DP-O	AC Coupled on Module
A38	GND	Power Ground	PWR GND	-
A39	PCIE_TX12+	PCI Express Lane 12 Transmit +	DP-O	AC Coupled on Module
A40	PCIE_TX12-	PCI Express Lane 12 Transmit -	DP-O	AC Coupled on Module
A41	GND	Power Ground	PWR GND	-
A42	USB2-	USB 2.0 Data Pair Port 2 –	DP-I/O	-
A43	USB2+	USB 2.0 Data Pair Port 2 +	DP-I/O	-
A44	USB_2_3_OC#	USB Overcurrent Indicator Port 2/3	I-3.3	PU 10k 3.3V (S5); Connected via 0R to USB_0_1_OC#
A45	USB0-	USB 2.0 Data Pair Port 0 –	DP-I/O	-
A46	USB0+	USB 2.0 Data Pair Port 0 +	DP-I/O	-
A47	VCC_RTC	Real-Time Clock Circuit Power Input	PWR 3V	Voltage range 2.0V to 3.3V (3.0V Nominal)
A48	RSVD	Reserved for future use	NC	-
A49	GBE0_SDP	Gigabit Eth. Controller 0 SW-Definable Pin	I/O-3.3 (S5)	-
A50	LPC_SERIRQ/ESPI_CS1 #	Serial Interrupt Request	I/OD-3.3	PU 8k2 3.3V (S0)

Pin	Signal	Description	Type	Termination / Comment
A51	GND	Power Ground	PWR GND	-
A52	PCIE_TX5+	PCI Express Lane 5 Transmit +	DP-O	AC Coupled on Module
A53	PCIE_TX5-	PCI Express Lane 5 Transmit -	DP-O	AC Coupled on Module
A54	GPI0	General Purpose Input 0	I-3.3	PU 100k 3.3V (S0)
A55	PCIE_TX4+	PCI Express Lane 4 Transmit +	DP-O	AC Coupled on Module
A56	PCIE_TX4-	PCI Express Lane 4 Transmit -	DP-O	AC Coupled on Module
A57	GND	Power Ground	PWR GND	-
A58	PCIE_TX3+	PCI Express Lane 3 Transmit +	DP-O	AC Coupled on Module
A59	PCIE_TX3-	PCI Express Lane 3 Transmit -	DP-O	AC Coupled on Module
A60	GND	Power Ground	PWR GND	-
A61	PCIE_TX2+	PCI Express Lane 2 Transmit +	DP-O	AC Coupled on Module
A62	PCIE_TX2-	PCI Express Lane 2 Transmit -	DP-O	AC Coupled on Module
A63	GPI1	General Purpose Input 1	I-3.3	PU 100k 3.3V (S0)
A64	PCIE_TX1+	PCI Express Lane 1 Transmit +	DP-O	AC Coupled on Module
A65	PCIE_TX1-	PCI Express Lane 1 Transmit -	DP-O	AC Coupled on Module
A66	GND	Power Ground	PWR GND	-
A67	GPI2	General Purpose Input 2	I-3.3	PU 100k 3.3V (S0)
A68	PCIE_TX0+	PCI Express Lane 0 Transmit +	DP-O	AC Coupled on Module
A69	PCIE_TX0-	PCI Express Lane 0 Transmit -	DP-O	AC Coupled on Module
A70	GND	Power Ground	PWR GND	-
A71	PCIE_TX8+	PCI Express Lane 8 Transmit +	DP-O	AC Coupled on Module
A72	PCIE_TX8-	PCI Express Lane 8 Transmit -	DP-O	AC Coupled on Module
A73	GND	Power Ground	PWR GND	-
A74	PCIE_TX9+	PCI Express Lane 9 Transmit +	DP-O	AC Coupled on Module
A75	PCIE_TX9-	PCI Express Lane 9 Transmit -	DP-O	AC Coupled on Module
A76	GND	Power Ground	PWR GND	-

Pin	Signal	Description	Type	Termination / Comment
A77	PCIE_TX10+	PCI Express Lane 10 Transmit +	DP-O	AC Coupled on Module
A78	PCIE_TX10-	PCI Express Lane 10 Transmit -	DP-O	AC Coupled on Module
A79	GND	Power Ground	PWR GND	-
A80	GND	Power Ground	PWR GND	-
A81	PCIE_TX11+	PCI Express Lane 11 Transmit +	DP-O	AC Coupled on Module
A82	PCIE_TX11-	PCI Express Lane 11 Transmit -	DP-O	AC Coupled on Module
A83	GND	Power Ground	PWR GND	-
A84	NCSI_TX_EN	NC-SI Transmit enable	I-3.3 (S5)	PD 10k
A85	GPI3	General Purpose Input 3	I-3.3	PU 100k 3.3V (S0)
A86	SPI_TPM_CS2_EXT#	SPI CS2 External Option	O-3.3/NC	Series 0R DNI
A87	RSVD	Reserved for future use	NC	-
A88	PCIE_CK_REF+	Reference PCI Express Clock +	DP-O	100MHz
A89	PCIE_CK_REF-	Reference PCI Express Clock -	DP-O	100MHz
A90	GND	Power Ground	PWR GND	-
A91	SPI_POWER	3.3V Power Output Pin for ext. SPI flash	O-3.3	100mA (max.)
A92	SPI_MISO	SPI Master IN Slave OUT	I-3.3	
A93	GPO0	General Purpose Output 0	O-3.3	PD 100k
A94	SPI_CLK	SPI Clock	O-3.3	
A95	SPI_MOSI	SPI Master Out Slave In	O-3.3	
A96	TPM_PP	TPM Physical Presence	I-3.3	PD 10k
A97	TYPE10#	Indicates TYPE10# to carrier board	NC	-
A98	SER0_TX	Serial Port 0 TXD	O-3.3	20V protection circuit implemented on module, PD on carrier needed for proper operation
A99	SER0_RX	Serial Port 0 RXD	I-5T	PU 10k 3.3V (S0); 20V protection circuit implemented on module
A100	GND	Power Ground	PWR GND	-
A101	SER1_TX	Serial Port 1 TXD	O-3.3	20V protection circuit implemented on module, PD on carrier needed for proper operation
A102	SER1_RX	Serial Port 1 RXD	I-5T	PU 10k 3.3V (S0); 20V protection circuit implemented on module

Pin	Signal	Description	Type	Termination / Comment
A103	LID#	LID Switch Input	I-3.3	PU 47k 3.3V (S5); 20V protection circuit implemented on module
A104	VCC_12V	Main Input Voltage	PWR	-
A105	VCC_12V	Main Input Voltage	PWR	-
A106	VCC_12V	Main Input Voltage	PWR	-
A107	VCC_12V	Main Input Voltage	PWR	-
A108	VCC_12V	Main Input Voltage	PWR	-
A109	VCC_12V	Main Input Voltage	PWR	-
A110	GND	Power Ground	PWR GND	-

Table 28: Pin-out List B

Pin	Signal	Description	Type	Termination / Comment
B1	GND	Power Ground	PWR GND	-
B2	GBE0_ACT#	Ethernet Activity LED	OD	-
B3	LPC_FRAME#/ESPI_CS0#	LPC Frame Indicator	O-3.3	-
B4	LPC_AD0/ESPI_IO_0	LPC Multiplexed Command, Addr & Data 0	I/O-3.3	-
B5	LPC_AD1/ESPI_IO_1	LPC Multiplexed Command, Addr & Data 1	I/O-3.3	-
B6	LPC_AD2/ESPI_IO_2	LPC Multiplexed Command, Addr & Data 2	I/O-3.3	-
B7	LPC_AD3/ESPI_IO_3	LPC Multiplexed Command, Addr & Data 3	I/O-3.3	-
B8	LPC_DRQ0#/ESPI_ALERT0#	LPC Serial DMA/Master Request 0	NC	Not supported
B9	LPC_DRQ1#/ESPI_ALERT1#	LPC Serial DMA/Master Request 1	NC	Not supported
B10	LPC_CLK/ESPI_CK	24MHz LPC clock	O-3.3	-
B11	GND	Power Ground	PWR GND	-
B12	PWRBTN#	Power Button	I-3.3	PU 10k 3.3V (S5)
B13	SMB_CK	SMBUS Clock	O-3.3	PU 3k3 3.3V (S5)
B14	SMB_DAT	SMBUS Data	I/O-3.3	PU 3k3 3.3V (S5)
B15	SMB_ALERT#	SMBUS Alert	I/O-3.3	PU 3k3 3.3V (S5)
B16	SATA1_TX+	SATA 1 Transmit Pair +	DP-O	AC Coupled on Module
B17	SATA1_TX-	SATA 1 Transmit Pair -	DP-O	AC Coupled on Module
B18	SUS_STAT#/ESPI_RESET#	Suspend Status	O-3.3	PD 10k
B19	SATA1_RX+	SATA 1 Receive Pair +	DP-I	AC Coupled on Module
B20	SATA1_RX-	SATA 1 Receive Pair -	DP-I	AC Coupled on Module

Pin	Signal	Description	Type	Termination / Comment
B21	GND	Power Ground	PWR GND	-
B22	PCIE_RX15+	PCI Express Lane 15 Receive +	DP-I	-
B23	PCIE_RX15-	PCI Express Lane 15 Receive -	DP-I	-
B24	PWR_OK	Power OK	I-3.3	PU 51K (S5) via diode
B25	PCIE_TX14+	PCI Express Lane 14 Receive +	DP-I	-
B26	PCIE_TX14-	PCI Express Lane 14 Receive -	DP-I	-
B27	WDT	Watch Dog Time-Out event	O-3.3	PD 10K
B28	R3.0: RSVD	Reserved for future use	NC	-
	R3.1: GND	Power Ground	PWR GND	-
B29	R3.0: RSVD	Reserved for future use	NC	-
	R3.1: PCIE1_CK_REF+	Reference PCI Express Clock+	DP-O	100MHz, for PCIe 4.0 on Lanes 16 to 31
B30	R3.0: RSVD	Reserved for future use	NC	-
	R3.1: PCIE1_CK_REF-	Reference PCI Express Clock-	DP-O	100MHz, for PCIe 4.0 on Lanes 16 to 31
B31	GND	Power Ground	PWR GND	-
B32	SPKR	Speaker	O-3.3	From FPGA
B33	I2C_CK	I2C Clock	O-3.3	PU 2k2 3.3V (S5)
B34	I2C_DAT	I2C Data	I/O-3.3	PU 2k2 3.3V (S5)
B35	THRM#	Over Temperature Input	I-3.3	PU 10k 3.3V (S0)
B36	PCIE_RX13+	PCI Express Lane 13 Receive +	DP-I	-
B37	PCIE_RX13-	PCI Express Lane 13 Receive -	DP-I	-
B38	GND	Power Ground	PWR GND	-
B39	PCIE_RX12+	PCI Express Lane 12 Receive +	DP-I	-
B40	PCIE_RX12-	PCI Express Lane 12 Receive -	DP-I	-
B41	GND	Power Ground	PWR GND	-
B42	USB3-	USB 2.0 Data Pair Port 3 –	DP-I/O	-
B43	USB3+	USB 2.0 Data Pair Port 3 +	DP-I/O	-
B44	USB_0_1_OC#	USB Overcurrent Indicator Port 0/1	I-3.3	PU 10k 3.3V (S5)
B45	USB1-	USB 2.0 Data Pair Port 1 –	DP-I/O	-
B46	USB1+	USB 2.0 Data Pair Port 1 +	DP-I/O	-

Pin	Signal	Description	Type	Termination / Comment
B47	ESPI_EN#	LPC/eSPI mode selection	NC	PU 20k 3.3V (S5); Not supported
B48	USB0_HOST_PRSNT	USB host presence on USB0	NC	Not supported
B49	SYS_RESET#	Reset Button Input	I-3.3	PU 10k 3.3V (S5)
B50	CB_RESET#	Carrier Board Reset	O-3.3	-
B51	GND	Power Ground	PWR GND	-
B52	PCIE_RX5+	PCI Express Lane 5 Receive +	DP-I	-
B53	PCIE_RX5-	PCI Express Lane 5 Receive -	DP-I	-
B54	GPO1	General Purpose Output 1	O-3.3	PD 100k
B55	PCIE_RX4+	PCI Express Lane 4 Receive +	DP-I	-
B56	PCIE_RX4-	PCI Express Lane 4 Receive -	DP-I	-
B57	GPO2	General Purpose Output 2	O-3.3	PD 100k
B58	PCIE_RX3+	PCI Express Lane 3 Receive +	DP-I	-
B59	PCIE_RX3-	PCI Express Lane 3 Receive -	DP-I	-
B60	GND	Power Ground	PWR GND	-
B61	PCIE_RX2+	PCI Express Lane 2 Receive +	DP-I	-
B62	PCIE_RX2-	PCI Express Lane 2 Receive -	DP-I	-
B63	GPO3	General Purpose Output 3	O-3.3	PD 100k
B64	PCIE_RX1+	PCI Express Lane 1 Receive +	DP-I	-
B65	PCIE_RX1-	PCI Express Lane 1 Receive -	DP-I	-
B66	WAKE0#	PCI Express Wake Event	I-3.3	PU 10k 3.3V (S5)
B67	WAKE1#	General Purpose Wake Event	I-3.3	PU 10k 3.3V (S5)
B68	PCIE_RX0+	PCI Express Lane 0 Receive +	DP-I	-
B69	PCIE_RX0-	PCI Express Lane 0 Receive -	DP-I	-
B70	GND	Power Ground	PWR GND	-
B71	PCIE_RX8+	PCI Express Lane 8 Receive +	DP-I	-
B72	PCIE_RX8-	PCI Express Lane 8 Receive -	DP-I	-
B73	GND	Power Ground	PWR GND	-
B74	PCIE_RX9+	PCI Express Lane 9 Receive +	DP-I	-
B75	PCIE_RX9-	PCI Express Lane 9 Receive -	DP-I	-
B76	GND	Power Ground	PWR GND	-
B77	PCIE_RX10+	PCI Express Lane 10 Receive +	DP-I	-
B78	PCIE_RX10-	PCI Express Lane 10 Receive -	DP-I	-
B79	GND	Power Ground	PWR GND	-
B80	GND	Power Ground	PWR GND	-

Pin	Signal	Description	Type	Termination / Comment
B81	PCIE_RX11+	PCI Express Lane 11 Receive +	DP-I	-
B82	PCIE_RX11-	PCI Express Lane 11 Receive -	DP-I	-
B83	GND	Power Ground	PWR GND	-
B84	VCC_5V_SBY	5V Standby	PWR 5V (S5)	optional (not necessary in single supply mode)
B85	VCC_5V_SBY	5V Standby	PWR 5V (S5)	optional (not necessary in single supply mode)
B86	VCC_5V_SBY	5V Standby	PWR 5V (S5)	optional (not necessary in single supply mode)
B87	VCC_5V_SBY	5V Standby	PWR 5V (S5)	optional (not necessary in single supply mode)
B88	BIOS_DIS1#	BIOS Selection Strap 1	I-3.3	PU 10k 3.3V (S5)
B89	NCSI_RX_ER	NC-SI Receive error	O-3.3	PD 10k DNI
B90	GND	Power Ground	PWR GND	-
B91	NCSI_CLK_IN	NC-SI Clock	I-3.3	PD 10k
B92	NCSI_RXD1	NC-SI Receive Data	O-3.3	-
B93	NCSI_RXD0	NC-SI Receive Data	O-3.3	-
B94	NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid	O-3.3	-
B95	NCSI_TXD1	NC-SI Transmit Data	I-3.3	PD 10k
B96	NCSI_TXD0	NC-SI Transmit Data	I-3.3	PD 10k
B97	SPI_CS#	SPI Chip Select	O-3.3	PU 4k7 (SPI)
B98	NCSI_ARB_IN	NC-SI hardware arbitration input	I-3.3	PD 10k
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output	O-3.3	PU 10k 3.3V (S5)
B100	GND	Power Ground	PWR GND	-
B101	FAN_PWMOUT	Fan PWM Output	O-3.3	20V protection circuit implemented on module, PD on carrier needed for proper operation
B102	FAN_TACHIN	Fan Tach Input	I-3.3	PU 47k 3.3V (S0); 20V protection circuit implemented on module
B103	SLEEP#	Sleep Button Input	I-3.3	PU 47k 3.3V (S5); 20V protection circuit implemented on module
B104	VCC_12V	Main Input Voltage	PWR	-
B105	VCC_12V	Main Input Voltage	PWR	-
B106	VCC_12V	Main Input Voltage	PWR	-
B107	VCC_12V	Main Input Voltage	PWR	-
B108	VCC_12V	Main Input Voltage	PWR	-
B109	VCC_12V	Main Input Voltage	PWR	-

Pin	Signal	Description	Type	Termination / Comment
B110	GND	Power Ground	PWR GND	-

Table 29: Pin-out List C

Pin	Signal	Description	Type	Termination / Comment
C1	GND	Power Ground	PWR GND	-
C2	GND	Power Ground	PWR GND	-
C3	USB_SSRX0-	USB Super Speed Receive – (0)	DP-I	-
C4	USB_SSRX0+	USB Super Speed Receive + (0)	DP-I	-
C5	GND	Power Ground	PWR GND	-
C6	USB_SSRX1-	USB Super Speed Receive – (1)	DP-I	-
C7	USB_SSRX1+	USB Super Speed Receive + (1)	DP-I	-
C8	GND	Power Ground	PWR GND	-
C9	USB_SSRX2-	USB Super Speed Receive – (2)	DP-I	-
C10	USB_SSRX2+	USB Super Speed Receive + (2)	DP-I	-
C11	GND	Power Ground	PWR GND	-
C12	USB_SSRX3-	USB Super Speed Receive – (3)	DP-I	-
C13	USB_SSRX3+	USB Super Speed Receive + (3)	DP-I	-
C14	GND	Power Ground	PWR GND	-
C15	R3.0: 10G_PHY_MDC_SCL3	Management I2C Clock for external PHY	O/OD-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
C16	R3.0: 10G_PHY_MDC_SCL2	Management I2C Clock for external PHY	O/OD-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
C17	10G_SDP2	Software-Definable Pin	I/O-3.3	-
C18	GND	Power Ground	PWR GND	-
C19	PCIE_RX6+	PCI Express Lane 6 Receive +	DP-I	-
C20	PCIE_RX6-	PCI Express Lane 6 Receive -	DP-I	-
C21	GND	Power Ground	PWR GND	-
C22	PCIE_RX7+	PCI Express Lane 7 Receive +	DP-I	-
C23	PCIE_RX7-	PCI Express Lane 7 Receive -	DP-I	-
C24	R3.0: 10G_INT2	Interrupt from copper PHY or optical SFP Module	I-3.3	PU 2k2 3.3V (S5)
	R3. 1: RSVD10G	Not used	NC	-
C25	GND	Power Ground	PWR GND	-

Pin	Signal	Description	Type	Termination / Comment
C26	10G_KR_RX3+	10GBASE-KR receive differential pair +	DP-I	AC Coupled on Module
C27	10G_KR_RX3-	10GBASE-KR receive differential pair -	DP-I	AC Coupled on Module
C28	GND	Power Ground	PWR GND	-
C29	10G_KR_RX2+	10GBASE-KR receive differential pair +	DP-I	AC Coupled on Module
C30	10G_KR_RX2-	10GBASE-KR receive differential pair -	DP-I	AC Coupled on Module
C31	GND	Power Ground	PWR GND	-
C32	R3.0: 10G_SFP_SDA3	Management I2C Data for optical SFP Module	I/O-3.3	PU 2k2 3.3V (S5)
	R3. 1: RSVD10G	Not used	NC	-
C33	R3.0: 10G_SFP_SDA2	Management I2C Data for optical SFP Module	I/O-3.3	PU 2k2 3.3V (S5)
	R3. 1: RSVD10G	Not used	NC	-
C34	R3.0: 10G_PHY_RST_23	Reset of optical PHY on ports 2 and 3	O-3.3	PD 10k
	R3. 1: RSVD10G	Not used	NC	-
C35	R3.0: 10G_PHY_RST_01	Reset of optical PHY on ports 0 and 1	O-3.3	PD 10k
	R3.1: CEI_RST#	Reset to I/O expander on carrier		
C36	R3.0: 10G_LED_SDA	I2C Data to transfer LED signals or MDIO of opt. PHY	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
C37	R3.0: 10G_LED_SCL	I2C Clock to transfer LED signals or MDIO of opt. PHY	O-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
C38	R3.0: 10G_SFP_SDA1	Management I2C Data for optical SFP Module	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
C39	R3.0: 10G_SFP_SDA0	Management I2C Data for optical SFP Module	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: CEI_SDA	I2C data – for SFP setup		PU 10k 3.3V (S5)
C40	10G_SDP0	Software-Definable Pin	I/O-3.3	-
C41	GND	Power Ground	PWR GND	-
C42	10G_KR_RX1+	10GBASE-KR receive differential pair +	DP-I	AC Coupled on Module
C43	10G_KR_RX1-	10GBASE-KR receive differential pair -	DP-I	AC Coupled on Module
C44	GND	Power Ground	PWR GND	-

Pin	Signal	Description	Type	Termination / Comment
C45	R3.0: 10G_PHY_MDC_SCL1	Management I2C Clock for external PHY	O/OD-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
C46	R3.0: 10G_PHY_MDC_SCL0	MDIO clock - for PHY setup	O/OD-3.3	PU 2k2 3.3V (S5)
	R3.1: CEI_MDC			PU 1k 3.3V (S5)
C47	R3.0: 10G_INT0	Interrupt from copper PHY or optical SFP Module	I-3.3	PU 2k2 3.3V (S5)
	R3.1: CEI_INT#	Interrupt from external I2C I/O expander		PU 10k 3.3V (S5)
C48	GND	Power Ground	PWR GND	-
C49	10G_KR_RX0+	10GBASE-KR receive differential pair +	DP-I	AC Coupled on Module
C50	10G_KR_RX0-	10GBASE-KR receive differential pair -	DP-I	AC Coupled on Module
C51	GND	Power Ground	PWR GND	-
C52	PCIE_RX16+	PCI Express Lane 16 Receive +	DP-I	-
C53	PCIE_RX16-	PCI Express Lane 16 Receive -	DP-I	-
C54	TYPE0#	GND for type 7 module	GND	-
C55	PCIE_RX17+	PCI Express Lane 17 Receive +	DP-I	-
C56	PCIE_RX17-	PCI Express Lane 17 Receive -	DP-I	-
C57	TYPE1#	NC for type 7 module	NC	-
C58	PCIE_RX18+	PCI Express Lane 18 Receive +	DP-I	-
C59	PCIE_RX18-	PCI Express Lane 18 Receive -	DP-I	-
C60	GND	Power Ground	PWR GND	-
C61	PCIE_RX19+	PCI Express Lane 19 Receive +	DP-I	-
C62	PCIE_RX19-	PCI Express Lane 19 Receive -	DP-I	-
C63	RSVD	Reserved for future use	NC	-
C64	RSVD	Reserved for future use	NC	-
C65	PCIE_RX20+	PCI Express Lane 20 Receive +	DP-I	-
C66	PCIE_RX20-	PCI Express Lane 20 Receive -	DP-I	-
C67	RAPID_SHUTDOWN	Trigger for Rapid Shutdown	I-5.0	PD 100k

Pin	Signal	Description	Type	Termination / Comment
C68	PCIE_RX21+	PCI Express Lane 21 Receive +	DP-I	-
C69	PCIE_RX21-	PCI Express Lane 21 Receive -	DP-I	-
C70	GND	Power Ground	PWR GND	-
C71	PCIE_RX22+	PCI Express Lane 22 Receive +	DP-I	-
C72	PCIE_RX22-	PCI Express Lane 22 Receive -	DP-I	-
C73	GND	Power Ground	PWR GND	-
C74	PCIE_RX23+	PCI Express Lane 23 Receive +	DP-I	-
C75	PCIE_RX23-	PCI Express Lane 23 Receive -	DP-I	-
C76	GND	Power Ground	PWR GND	-
C77	RSVD	Reserved for future use	NC	-
C78	PCIE_RX24+	PCI Express Lane 24 Receive +	DP-I	-
C79	PCIE_RX24-	PCI Express Lane 24 Receive -	DP-I	-
C80	GND	Power Ground	PWR GND	-
C81	PCIE_RX25+	PCI Express Lane 25 Receive +	DP-I	-
C82	PCIE_RX25-	PCI Express Lane 25 Receive -	DP-I	-
C83	RSVD	Reserved for future use	NC	-
C84	GND	Power Ground	PWR GND	-
C85	PCIE_RX26+	PCI Express Lane 26 Receive +	DP-I	-
C86	PCIE_RX26-	PCI Express Lane 26 Receive -	DP-I	-
C87	GND	Power Ground	PWR GND	-
C88	PCIE_RX27+	PCI Express Lane 27 Receive +	DP-I	-
C89	PCIE_RX27-	PCI Express Lane 27 Receive -	DP-I	-
C90	GND	Power Ground	PWR GND	-
C91	PCIE_RX28+	PCI Express Lane 28 Receive +	DP-I	-
C92	PCIE_RX28-	PCI Express Lane 28 Receive -	DP-I	-
C93	GND	Power Ground	PWR GND	-

Pin	Signal	Description	Type	Termination / Comment
C94	PCIE_RX29+	PCI Express Lane 29 Receive +	DP-I	-
C95	PCIE_RX29-	PCI Express Lane 29 Receive -	DP-I	-
C96	GND	Power Ground	PWR GND	-
C97	RSVD	Reserved for future use	NC	-
C98	PCIE_RX30+	PCI Express Lane 30 Receive +	DP-I	-
C99	PCIE_RX30-	PCI Express Lane 30 Receive -	DP-I	-
C100	GND	Power Ground	PWR GND	-
C101	PCIE_RX31+	PCI Express Lane 31 Receive +	DP-I	-
C102	PCIE_RX31-	PCI Express Lane 31 Receive -	DP-I	-
C103	GND	Power Ground	PWR GND	-
C104	VCC_12V	Main Input Voltage	PWR	-
C105	VCC_12V	Main Input Voltage	PWR	-
C106	VCC_12V	Main Input Voltage	PWR	-
C107	VCC_12V	Main Input Voltage	PWR	-
C108	VCC_12V	Main Input Voltage	PWR	-
C109	VCC_12V	Main Input Voltage	PWR	-
C110	GND	Power Ground	PWR GND	-

Table 30: Pin-out List D

Pin	Signal	Description	Type	Termination / Comment
D1	GND	Power Ground	PWR GND	-
D2	GND	Power Ground	PWR GND	-
D3	USB_SSTX0-	USB Super Speed Transmit – (0)	DP-O	-
D4	USB_SSTX0+	USB Super Speed Transmit + (0)	DP-O	-
D5	GND	Power Ground	PWR GND	-
D6	USB_SSTX1-	USB Super Speed Transmit – (1)	DP-O	-
D7	USB_SSTX1+	USB Super Speed Transmit + (1)	DP-O	-
D8	GND	Power Ground	PWR GND	-
D9	USB_SSTX2-	USB Super Speed Transmit – (2)	DP-O	-

Pin	Signal	Description	Type	Termination / Comment
D10	USB_SSTX2+	USB Super Speed Transmit + (2)	DP-O	-
D11	GND	Power Ground	PWR GND	-
D12	USB_SSTX3-	USB Super Speed Transmit – (3)	DP-O	-
D13	USB_SSTX3+	USB Super Speed Transmit + (3)	DP-O	-
D14	GND	Power Ground	PWR GND	-
D15	R3.0: 10G_PHY_MDIO_SDA3	Management I2C Data for external PHY	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
D16	R3.0: 10G_PHY_MDIO_SDA2	Management I2C Data for external PHY	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
D17	10G_SDP3	Software-Definable Pin	I/O-3.3	-
D18	GND	Power Ground	PWR GND	-
D19	PCIE_TX6+	PCI Express Lane 6 Transmit +	DP-O	AC Coupled on Module
D20	PCIE_TX6-	PCI Express Lane 6 Transmit -	DP-O	AC Coupled on Module
D21	GND	Power Ground	PWR GND	-
D22	PCIE_TX7+	PCI Express Lane 7 Transmit +	DP-O	AC Coupled on Module
D23	PCIE_TX7-	PCI Express Lane 7 Transmit -	DP-O	AC Coupled on Module
D24	R3.0: 10G_INT3	Interrupt From copper PHY or optical SFP Module	I-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
D25	GND	Power Ground	PWR GND	-
D26	10G_KR_TX3+	10GBASE-KR Transmit +	DP-O	-
D27	10G_KR_TX3-	10GBASE-KR Transmit -	DP-O	-
D28	GND	Power Ground	PWR GND	-
D29	10G_KR_TX2+	10GBASE-KR Transmit +	DP-O	-
D30	10G_KR_TX2-	10GBASE-KR Transmit -	DP-O	-
D31	GND	Power Ground	PWR GND	-
D32	R3.0: 10G_SFP_SCL3	Management I2C Clock for optical SFP Module	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
D33	R3.0: 10G_SFP_SCL2	Management I2C Clock for optical SFP Module	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-

Pin	Signal	Description	Type	Termination / Comment
D34	R3.0: 10G_PHY_CAP_23	PHY on ports 2 and 3 mode capability – I2C or MDIO	I-3.3	PU 10k 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
D35	R3.0: 10G_PHY_CAP_01	PHY on ports 0 and 1 mode capability – I2C or MDIO	I-3.3	PU 10k 3.3V (S5)
	R3.1: CEI_PRSNT#	Presence of CEI compliant hardware		
D36	RSVD	Reserved for future use	NC	-
D37	RSVD	Reserved for future use	NC	-
D38	R3.0: 10G_SFP_SCL1	Management I2C Clock for optical SFP Module	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
D39	R3.0: 10G_SFP_SCL0	Management I2C Clock for optical SFP Module	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: CEI_SCL	I2C clock for CEI I2C port		PU 10k 3.3V (S5)
D40	10G_SDP1	Software-Definable Pin	I/O-3.3	-
D41	GND	Power Ground	PWR GND	-
D42	10G_KR_TX1+	10GBASE-KR Transmit +	DP-O	-
D43	10G_KR_TX1-	10GBASE-KR Transmit -	DP-O	-
D44	GND	Power Ground	PWR GND	-
D45	R3.0: 10G_PHY_MDIO_SDA1	Management I2C Data for external PHY	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: RSVD10G	Not used	NC	-
D46	R3.0: 10G_PHY_MDIO_SDA0	MDIO data – for external PHY setup	I/O-3.3	PU 2k2 3.3V (S5)
	R3.1: CEI_MDIO			PU 1k 3.3V (S5)
D47	R3.0: 10G_INT1	Interrupt from copper PHY or optical SFP Module	I-3.3	PU 2k2 3.3V (S5)
	R3.1: ETH_PHY_INT#	Interrupt from external I2C I/O expander		PU 2k 3.3V (S5)
D48	GND	Power Ground	PWR GND	-
D49	10G_KR_TX0+	10GBASE-KR Transmit +	DP-O	-
D50	10G_KR_TX0-	10GBASE-KR Transmit -	DP-O	-
D51	GND	Power Ground	PWR GND	-
D52	PCIE_TX16+	PCI Express Lane 16 Transmit +	DP-O	AC Coupled on Module
D53	PCIE_TX16-	PCI Express Lane 16 Transmit -	DP-O	AC Coupled on Module
D54	RSVD	Reserved for future use	NC	-
D55	PCIE_TX17+	PCI Express Lane 17 Transmit +	DP-O	AC Coupled on Module

Pin	Signal	Description	Type	Termination / Comment
D56	PCIE_TX17-	PCI Express Lane 17 Transmit -	DP-O	AC Coupled on Module
D57	TYPE2#	GND for type 7 module	GND	-
D58	PCIE_TX18+	PCI Express Lane 18 Transmit +	DP-O	AC Coupled on Module
D59	PCIE_TX18-	PCI Express Lane 18 Transmit -	DP-O	AC Coupled on Module
D60	GND	Power Ground	PWR GND	-
D61	PCIE_TX19+	PCI Express Lane 19 Transmit +	DP-O	AC Coupled on Module
D62	PCIE_TX19-	PCI Express Lane 19 Transmit -	DP-O	AC Coupled on Module
D63	RSVD	Reserved for future use	NC	-
D64	RSVD	Reserved for future use	NC	-
D65	PCIE_TX20+	PCI Express Lane 20 Transmit +	DP-O	AC Coupled on Module
D66	PCIE_TX20-	PCI Express Lane 20 Transmit -	DP-O	AC Coupled on Module
D67	GND	Power Ground	PWR GND	-
D68	PCIE_TX21+	PCI Express Lane 21 Transmit +	DP-O	AC Coupled on Module
D69	PCIE_TX21-	PCI Express Lane 21 Transmit -	DP-O	AC Coupled on Module
D70	GND	Power Ground	PWR GND	-
D71	PCIE_TX22+	PCI Express Lane 22 Transmit +	DP-O	AC Coupled on Module
D72	PCIE_TX22-	PCI Express Lane 22 Transmit -	DP-O	AC Coupled on Module
D73	GND	Power Ground	PWR GND	-
D74	PCIE_TX23+	PCI Express Lane 23 Transmit +	DP-O	AC Coupled on Module
D75	PCIE_TX23-	PCI Express Lane 23 Transmit -	DP-O	AC Coupled on Module
D76	GND	Power Ground	PWR GND	-
D77	RSVD	Reserved for future use	NC	-
D78	PCIE_TX24+	PCI Express Lane 24 Transmit +	DP-O	AC Coupled on Module
D79	PCIE_TX24-	PCI Express Lane 24 Transmit -	DP-O	AC Coupled on Module
D80	GND	Power Ground	PWR GND	-
D81	PCIE_TX25+	PCI Express Lane 25 Transmit +	DP-O	AC Coupled on Module

Pin	Signal	Description	Type	Termination / Comment
D82	PCIE_TX25-	PCI Express Lane 25 Transmit -	DP-O	AC Coupled on Module
D83	RSVD	Reserved for future use	NC	-
D84	GND	Power Ground	PWR GND	-
D85	PCIE_TX26+	PCI Express Lane 26 Transmit +	DP-O	AC Coupled on Module
D86	PCIE_TX26-	PCI Express Lane 26 Transmit -	DP-O	AC Coupled on Module
D87	GND	Power Ground	PWR GND	-
D88	PCIE_TX27+	PCI Express Lane 27 Transmit +	DP-O	AC Coupled on Module
D89	PCIE_TX27-	PCI Express Lane 27 Transmit -	DP-O	AC Coupled on Module
D90	GND	Power Ground	PWR GND	-
D91	PCIE_TX28+	PCI Express Lane 28 Transmit +	DP-O	AC Coupled on Module
D92	PCIE_TX28-	PCI Express Lane 28 Transmit -	DP-O	AC Coupled on Module
D93	GND	Power Ground	PWR GND	-
D94	PCIE_TX29+	PCI Express Lane 29 Transmit +	DP-O	AC Coupled on Module
D95	PCIE_TX29-	PCI Express Lane 29 Transmit -	DP-O	AC Coupled on Module
D96	GND	Power Ground	PWR GND	-
D97	RSVD	Reserved for future use	NC	-
D98	PCIE_TX30+	PCI Express Lane 30 Transmit +	DP-O	AC Coupled on Module
D99	PCIE_TX30-	PCI Express Lane 30 Transmit -	DP-O	AC Coupled on Module
D100	GND	Power Ground	PWR GND	-
D101	PCIE_TX31+	PCI Express Lane 31 Transmit +	DP-O	AC Coupled on Module
D102	PCIE_TX31-	PCI Express Lane 31 Transmit -	DP-O	AC Coupled on Module
D103	GND	Power Ground	PWR GND	-
D104	VCC_12V	Main Input Voltage	PWR	-
D105	VCC_12V	Main Input Voltage	PWR	-
D106	VCC_12V	Main Input Voltage	PWR	-
D107	VCC_12V	Main Input Voltage	PWR	-
D108	VCC_12V	Main Input Voltage	PWR	-
D109	VCC_12V	Main Input Voltage	PWR	-
D110	GND	Power Ground	PWR GND	-

Table 31: Summary – COM.0 REV3.1 vs REV3.0

REV3.1	REV 3.1 Description	REV3.0	Pin
GBE0_LINK_MID#	Gigabit Ethernet Controller MID Speed Link indicator	GBE0_LINK_100#	A4
GBE0_LINK_MAX#	Gigabit Ethernet Controller MAX Speed Link indicator	GBE0_LINK_1000#	A5
PCIE1_CK_REF+ PCIE1_CK_REF-	Second reference clock output for higher speed PCI Express implementation on Lanes 16 to 31	Reserved pins	B29 B30
CEI_MDIO	MDIO data – for PHY setup	10G_PHY_MDIO_SDA0	D46
CEI_MDC	MDIO clock - for PHY setup	10G_PHY_MDC_SCL0	C46
CEI_SDA	I2C data – for SFP setup, serialized status LEDs and miscellaneous serialized signals	10G_SFP_SDA0	C39
CEI_SCL	I2C clock for CEI I2C port	10G_SFP_SCL0	D39
CEI_INT#	Active low interrupt input to Module from Carrier based I2C I/O expander	10G_INT0	C47
ETH_PHY_INT#	Second active low interrupt input to Module from Carrier based I2C I/O expander	10G_INT1	D47
CEI_RST#	Active low reset output from Module to Carrier based I/O expander	10G_PHY_RST_01	C35
CEI_PRSNT#	Input signal from Carrier indicating presence of CEI compliant hardware on the Carrier	10G_PHY_CAP_01	D35
Reserved pin	Not used	10G_PHY_RST_23	C34
Reserved pin	Not used	10G_PHY_CAP_23	D34
Reserved pins	Not used	10G_PHY_MDIO_SDA[1:3]	D45, D16, D15
Reserved pins	Not used	10G_PHY_MDC_SCL[1:3]	C45, C16, C15
Reserved pins	Not used	10G_SFP_SDA[1:3]	C38, C33, C32
Reserved pins	Not used	10G_SFP_SCL[1:3]	D38, D33, D32
Reserved pin	Not used	10G_LED_SDA	C36
Reserved pin	Not used	10G_LED_SCL	C37
Reserved pins	Not used	10G_INT[2:3]	C24, D24

11/ UEFI BIOS

11.1. Starting the UEFI BIOS

The COMe-bID7 uses a Kontron-customized, pre-installed and configured version AMI EFI BIOS Aptio ® V based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI. This UEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the COMe-bDV7.

i The BIOS version covered in this document might not be the latest version. The latest version might have certain differences to the BIOS options and features described in this chapter.

i Register for the EMD Customer Section to access BIOS downloads and the Product Change Notification (PCN) service at Kontron's Customer Section.

The UEFI BIOS comes with a Setup program that provides quick and easy access to the individual function settings for control or modification of the UEFI BIOS configuration. The Setup program allows for access to various menus that provide functions or access to sub-menus with further specific functions of their own.

To start the UEFI BIOS Setup program, follow the steps below:

1. Power on the board.

Wait until the first characters appear on the screen (POST messages or splash screen).

Press the <DEL> key.

If the UEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see

Security Setup Menu), press <RETURN>, and proceed with step 5.

A Setup menu appears.

The COMe-bID7 UEFI BIOS Setup program uses a hot key navigation system. The hot key legend bar is located at the bottom of the Setup screens. The following table provides a list of navigation hot keys available in the legend bar.

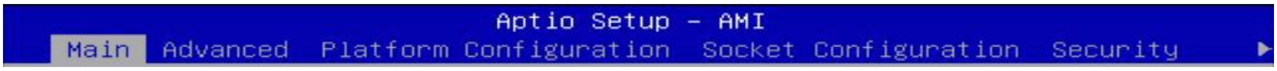
Table 32: Navigation Hot Keys Available in the Legend Bar

Sub-screen	Description
<F1>	<F1> key invokes the General Help window
<->	<Minus> key selects the next lower value within a field
<+>	<Plus> key selects the next higher value within a field
<F2>	<F2> key loads previous values
<F3>	<F3> key loads optimized defaults
<F4>	<F4> key Saves and Exits
<→> or <←>	<Left/Right> arrows selects major Setup menus on menu bar, for example, Main or Advanced
<↑> or <↓>	<Up/Down> arrows select fields in the current menu, for example, Setup function or sub-screen
<ESC>	<ESC> key exits a major Setup menu and enters the Exit Setup menu Pressing the <ESC> key in a sub-menu displays the next higher menu level
<RETURN>	<RETURN> key executes a command or selects a submenu

11.2. Setup Menus

The Setup utility features a selection bar at the top of the screen that lists the menus.

Figure 12: Setup Menu Selection Bar



The Setup menus available for the COMe-bID7 are:

- Main
- Advanced
- PlatformConfiguration
- Socket Configuration
- Security
- Boot
- Save & Exit

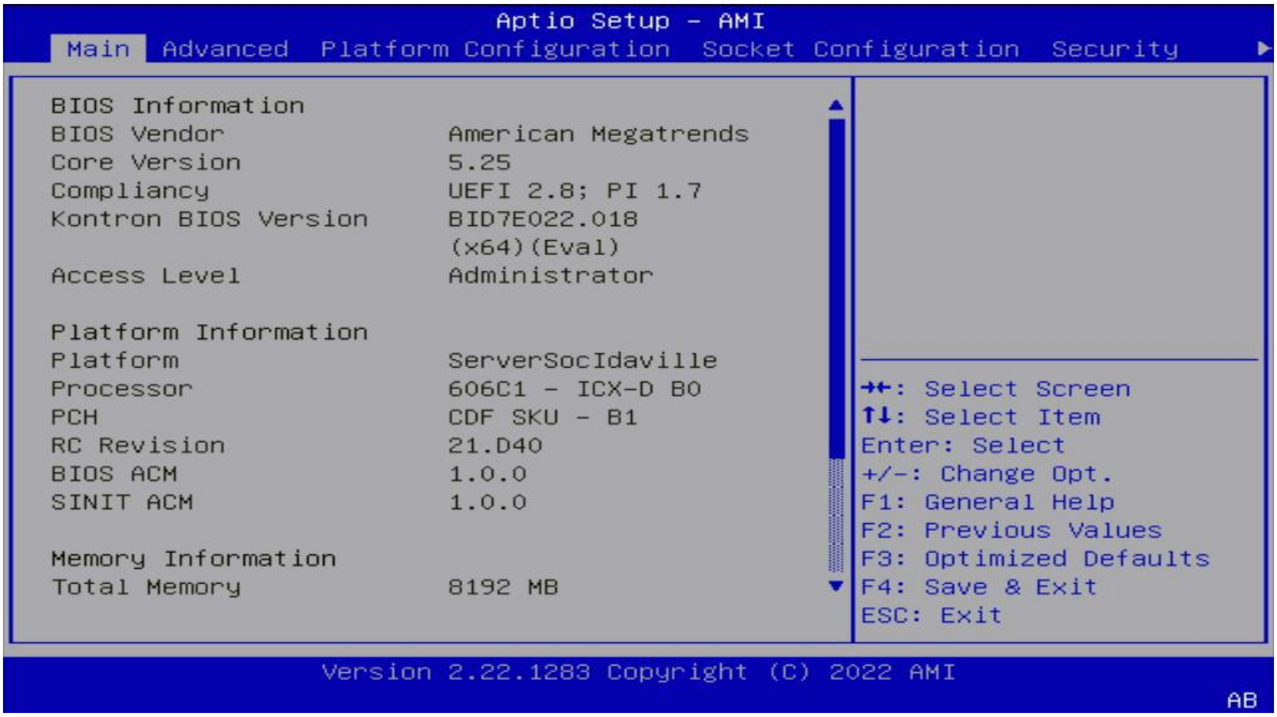
The currently active menu and the currently active UEFI BIOS Setup item are highlighted in white. Use the left and right arrow keys to select the Setup menus.

Each Setup menu provides two main frames. The left frame displays all available functions. Configurable functions are displayed in blue. Functions displayed in grey provide information about the status or the operational configuration. The right frame displays a Help window providing an explanation of the respective function.

11.3. Main Menu

On entering the UEFI BIOS, the Setup program displays the Main Setup menu that lists basic system information.

Figure 13: Main Setup Menu



```
BIOS Information
BIOS Vendor                 American Megatrends
Core Version                5.25
Compliancy                  UEFI 2.8; PI 1.7
Kontron BIOS Version        BID7E022.018
                            (x64)(Eval)
Access Level                Administrator

Platform Information
Platform                    ServerSocIdaville
Processor                   606C1 - ICX-D B0
PCH                         CDF SKU - B1
RC Revision                 21.D40
BIOS ACM                    1.0.0
SINIT ACM                   1.0.0

Memory Information
Total Memory                8192 MB
```

The following table shows Main sub-screens and functions, and describes the content. Default settings are in **bold**. Some function contain additional information

Table 33: Main Setup Menu Sub-screens

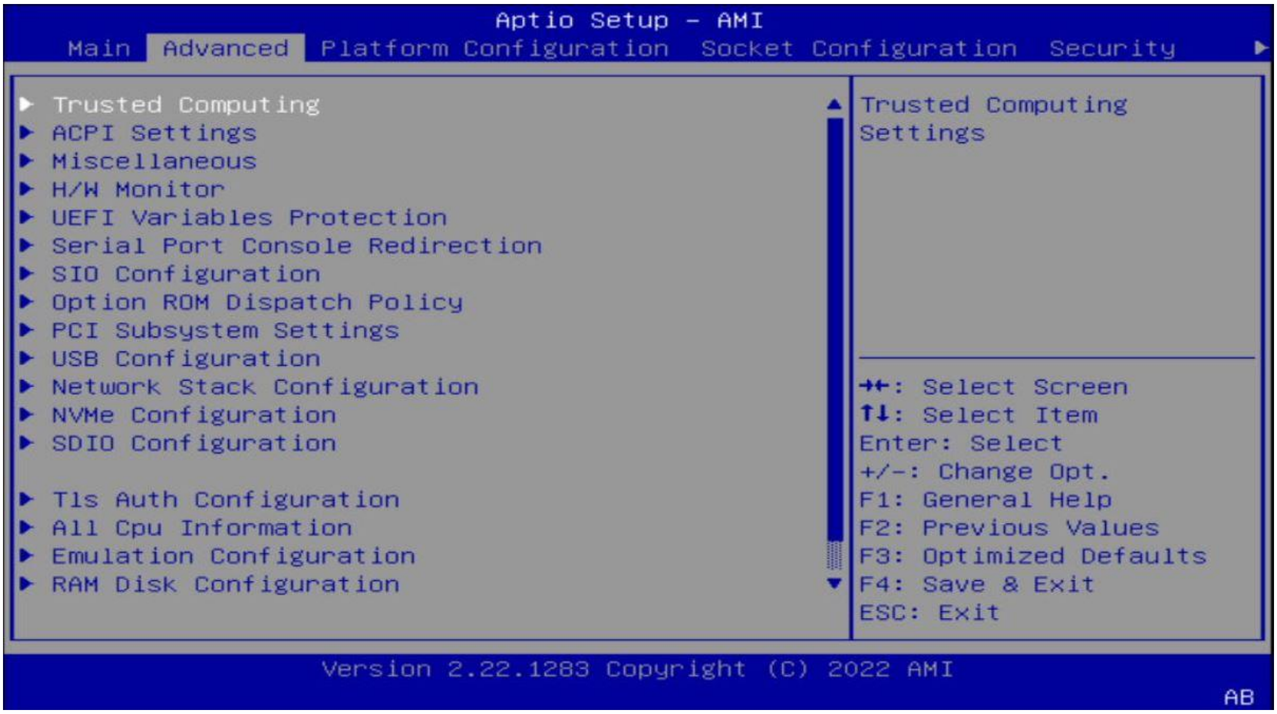
Sub-Screen	Description
BIOS Information	Read only field BIOS Vendor, Core Version, Compliancy, Kontron BIOS Version, Access Level
Platform Information	Read only field Platform, Processor, PCH, RC revision, BIOS ACM, SINIT ACM
Memory Information	Read only field Total memory
System Language	Selects system default language [**English**]
System Date	Displays the system date [Week Day mm/dd/yyyy]
Platform Information	Product Name, Revision, Serial #, MAC Address, Boot Counter, CPLD Rev
System Date	Displays the system time [hh:mm:ss]

11.4. Advanced Setup Menu

The Advanced Setup menu provides sub-screens and second level sub-screens with functions, for advanced configuration and Kontron specific configurations.

NOTICE Setting items on this screen to incorrect values may cause system malfunctions.

Figure 14: Advanced Setup Menu



```
                                Aptio Setup - AMI
    Main  Advanced  Platform Configuration  Socket Configuration  Security  ►

 ► Trusted Computing                                  ▲ Trusted Computing
 ► ACPI Settings                                        Settings
 ► Miscellaneous
 ► H/W Monitor
 ► UEFI Variables Protection
 ► Serial Port Console Redirection
 ► SIO Configuration
 ► Option ROM Dispatch Policy
 ► PCI Subsystem Settings
 ► USB Configuration
 ► Network Stack Configuration                          →←: Select Screen
 ► NVMe Configuration                                   ↑↓: Select Item
 ► SDIO Configuration                                   Enter: Select
                                                        +/-: Change Opt.
 ► Tls Auth Configuration                               F1: General Help
 ► All Cpu Information                                  F2: Previous Values
 ► Emulation Configuration                              F3: Optimized Defaults
 ► RAM Disk Configuration                             ▼ F4: Save & Exit
                                                        ESC: Exit

                    Version 2.22.1283 Copyright (C) 2022 AMI
                                                                            AB
```

The following table provides an over view of the Advanced menu sub-screens and functions listed below and describes the content. Default settings are in **bold**. Some function contain additional information

Table 34: Advanced Setup menu Sub-screens and Functions

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description	
Trusted Computing	Security device Support	Enables or disables BIOS support for security device. Operating System will not show security device. The TCG EFI protocol and INT1A interface are not available. [**Enabled**, Disabled]	
	Active PCR Banks	[**SHA-1**]	
	Available PCR Banks	[**SHA-1, SHA256**]	
	SHA-1 PCR Bank	[**Enable**/Disable]	
	SHA256 PCR Bank	[**Enable**/Disable]	
	Pending Operation	Schedules an operation for Security Device Note: Computer reboots on restart in order to change the state of the security device. [**None**, TPM Clear]	
	Platform Hierarchy	[**Enabled**, Disabled]	
	Storage Hierarchy	[**Enabled**, Disabled]	
	Endorsement Hierarchy	[**Enabled**, Disabled]	
	TPM2.0 UEFI Spec Version	Selects TCG2 Spec Version support: TCG_1_2 -compatible mode for Win8/Win10 and TCG_2: supports TCG2 protocol and event format for Win10 or later. [TCG_1_2, **TCG_2**]	
	Physical Presence Spec Version	Select to tell OS to support either PPI Spec 1.2 or 1.3 Note: Some HCK tests might not support 1.3. [1.2, **1.3**]	
	TPM 20 InterfaceType	Read only field [TIS]	
	Device Select	BIOS support for security devices. Auto supports both TPM 1.2 and TPM 2.0. TPM 1.2 supports TPM 1.2 devices only and TPM 2.0 supports TPM 2.0. devices only. [TPM 1.2, TPM 2.0, **Auto**]	
ACPI Settings	Enable ACPI Auto Configuration	Enables or disables ACPI auto configuration. If enabled, the system uses generic ACPI settings that may not fit the system best. [Enabled, **Disabled**]	
Miscellaneous	Generic eSPI Decode Ranges	Generic LPC via eSPI	Enables or disables the generic LPC via aSPI decode range [Enabled, **Disabled**]
	Watchdog	Auto Reload	Enables automatic reload of watchdog timers on timeout [Enabled, **Disabled**]

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description	
		Global Lock	If set to Enabled, all Watchdog registers (except for WD_KICK) to read only until board is reset. [Enabled, **Disabled**]
		Stage 1 Mode	Selects action for this Watchdog stage [**Disabled**, Reset, Delay, WDT Signal only]
	Reset Button Behavior	Selects reset button behavior [**Chipset Reset**, Power Cycle]	
	I2C Speed	Selects internal I2C bus speed between (1 kHz and 400 kHz) For a default system 200kHz is appropriate.	
	Onboard I2C Mode	[**MultiMaster**, BusClear]	
	Manufacturing Mode	Read only field [**Enabled**]	
	BIOS Test Mode	[**Disabled**]	
	ACPI temperature polling	[**Enabled**, Disabled	
	TZ00 temperature polling time	30	
	Create ACPI AC adaptor	[**Enabled**, Disabled]	
	SMBus device ACPI mode	[**Normal,** Hidden]	
	CPLD device ACPI mode	[**Normal,** Hidden]	
	SPI lines active	[**SPIO,** GSPIO]	
	Control COMe GPIOs in BIOS	[Enabled, **Disabled**]	
	GPIO IRQ #	[Enabled, **Disabled**]	
	I2C IRQ #	[Enabled, **Disabled**]	
	Local FW Update	[**Enabled**, Disabled]	
H/W Monitor	CPU Temperature, Module Temperature		
	CPU Temperature	Read only field Displays CPU temperature in °C	
	CPU Fan – Fan Control	Set fan control mode. 'Disable' will totally stop the fan. ▶ Disable - stops fan. ▶ Manual – manually sets the fan. ▶ Auto – Hardware monitor controls cooling, similar to ACPI based 'Active Cooling', without producing a software load to the system. [Disable, Manual, **Auto**]	
	CPU Fan – Fan Pulse	Displays number of pulses fan produces during 1 revolution. (Range: 1-4) [**2**]	

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description
	CPU Fan – Fan Trip Point	Displays temperature at which the fan accelerates. (Range: 20°C – 80°) [**50**]
	CPU Fan – Trip Point Speed	Displays Fan speed at trip point in %. Minimum value is 30 %. Fan always runs at 100 % at TJmax (-10°C). [**50**]
	CPU Fan – Ref. Temperature	Determines temperature source used for automatic fan control [PCH Temperature, Module Temperature, **CPU Temperature**]
	External Fan-Fan Control	Set fan control mode. 'Disable' will totally stop the fan. a. Disable - stops fan. b. Manual – manually sets the fan. c. Auto – Hardware monitor controls cooling, similar to ACPI based 'Active Cooling', without producing a software load to the system. [Disable, Manual, **Auto**]
	External Fan–Fan Pulse	Displays number of pulse fan produces during 1 revolution (Range: 1-4) [**2**]
	External Fan-Fan Trip point	Displays temperature at which fan accelerates. (Range: 20°C to 80°C) [**50**]
	External Fan-Trip Point Speed	Displays Fan speed at trip point in %. Minimum value is 30% Fan always runs at 100% at TJmax (-10°C) [**50**]
	Fan Reference Temperature	Determines temperature source used for automatic fan control [PCH Temperature, Module Temperature, **CPU Temperature**]
	5.0 V Standby	Read only field Displays standby voltage
	Batt Volt. at COMe Pin	Read only field Displays battery voltage at COMe pin
	Widerange Vcc	Read only field Displays wide range VCC
UEFI Variables Protection	Password protection of Runtime Variables	[Enabled, **Disabled**]
Serial Port Console Redirection	COM1 Console Redirection Settings	Console redirection via COMe module's COM1. If redirection is enabled then the port settings such as Terminal type, Bits per second, Data bits, Parity etc. can be adjusted here. Note: On-module COM ports do not support flow control. [**Enabled**, Disabled]
	COM1 Console Redirection settings	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description	
		Terminal Type	Emulation: ANSI: Extended ASCII character set VT100: ASCII character set VT100+: Extend VT100 to support color, function keys etc. VT-UTF8: uses UTF8 encoding to map Unicode chars onto 1 or more bytes. [VT100, VT100+, VT-UTF8, **ANSI**]
		Bits per Second	Selects the serial port transmission speed. The sped must be matched on the other side. Long or noisy lines may require lower speeds. [9600, 19200, 38400, 57600, **115200**]
		Data Bits	Data Bits [7, **8**]
		Parity	A parity bit can be sent with the data bits to detect transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow error detection. [**None** , Even, Odd, Mark, Space]
		Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. [**1**, 2]
		Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. [**None**, hardware RTS/CTS]
		VT-UTF8 Combo Key Support	Enables VT-UTF8 combination key support for ANSI/VT100 terminals [**Enabled**, Disabled]
		Recorder Mode	If enabled, only text will be sent. This is to capture terminal data. [Enabled, **Disabled**]
		Resolution 100x31	Enables or disables extended terminal resolution. [Enabled, **Disabled**]
		Legacy OS Redirection Resolution	On legacy OS, the number of row and columns supported redirection [**80x24**, 80x25]

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description	
		Putty Keypad	Select function key and key pad on putty. [**VT100**, LINUX, XTERMR6, SCO, ESCN, VT400]
	COM2 Console Redirection	Console redirection via COMe module's COM2. If redirection is enabled then the port settings such as Terminal type, Bits per second, Data bits, Parity etc. can be adjusted here. Note: On-module COM ports do not support flow control. [Enabled, **Disabled**]	
	COM2 Console Redirection settings	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.	
		Terminal Type	Emulation: ANSI: Extended ASCII character set VT100: ASCII character set VT100+: Extend VT100 to support color, function keys etc. VT-UTF8: uses UTF8 encoding to map Unicode chars onto 1 or more bytes. [VT100, VT100+, VT-UTF8, ANSI]
		Bits per Second	Selects the serial port transmission speed. The sped must be matched on the other side. Long or noisy lines may require lower speeds. [9600, 19200, 38400, 57600, 115200]
		Data Bits	Data Bits [7, 8]
		Parity	A parity bit can be sent with the data bits to detect transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow error detection. [None , Even, Odd, Mark, Space]
		Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. [1, 2]

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description	
		Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. [None, hardware RTS/CTS]
		VT-UTF8 Combo Key Sup	Enables VT-UTF8 combination key support for ANSI/VT100 terminals [Enabled, Disabled]
		Recorder Mode	If enabled, only text will be sent. This is to capture terminal data. [Enabled, Disabled]
		Resolution 100x31	Enables or disables extended terminal resolution. [Enabled, Disabled]
		Legacy OS Redirecton Resolution	On legacy OS, the number of row and columns supported redirection [80x24, 80x25]
		Putty Keypad	Select function key and key pad on putty. [VT100, LINUX, XTERMR6, SCO, ESCN, VT400]
	Legacy Console Redirection Settings	Legacy Serial Redirection Port	Selects a COM port to display redirection of legacy OS and legacy OPROM messages [**COM0**, COM1]
		Resolution	[**80x24**, 80x25]
		Redirection after POST	[Always enable, Bootloader]
	Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS) - Console Redirection EMS	Console redirection EMS [**Enabled**, Disabled]	
	Console Redirection Settings	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.	
		Out-of-Band Mgmt Port	Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description	
			[**COM0**, COM1]
		Terminal Type	VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation. [VT100, VT100+, **VT-UTF8**, ANSI]
		Bits per second	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds. [9600, 19200, 57600, **115200**]
		Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. [**None**, Hardware RTS/CTS, Software Xon/Xoff]
SIO Configuration	Read only field AMI SIO Driver Version		
	Serial Port 0	Use This Device	Enables the user to change the device's resource settings. New setting will be reflected on this setup page after system restart. [**Enabled**, Disabled]
		Logical Device Settings Current	Read only field
		Possible	Allows the user to change the device's resource settings. New settings are reflected on the Setup page after system restarts. [**Use Automatic Settings**]
	Read Only field WARNING: Disabling SIO Logical Devices may have unwanted side effects. PROCEED WITH CAUTION.		
	Serial Port 1	Use This Device	Enables the user to change the device's resource settings. New setting will be reflected on this setup page after system restart. [**Enabled**, Disabled]
		Logical Device Settings Current	Read only field
		Possible	Allows the user to change the device's resource settings. New settings are reflected on the Setup page after system restarts.

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description	
			[**Use Automatic Settings**]
	Read only field WARNING: Disabling SIO Logical Devices may have unwanted side effects. PROCEED WITH CAUTION.		
Option ROM Dispatch Policy	Restore if Failure	[**Enabled**, Disabled]	
	Primary Video Ignore	[**Enabled**, Disabled]	
	On Board Network	[**Enabled**, Disabled]	
	Controller Slot #x	[**Enabled**, Disabled]	
PCI Subsystem Settings	Read only field PCI Bus Driver version		
	PCI Latency Timer	Displays value to be programmed into the PCI latency timer register [**32**, 64, 96, 128, 160, 192, 224, 248]	
	PCI-X Latency Timer	Displays value to be programmed into the PCI latency timer register [32, **64**, 96, 128, 160, 192, 224, 248]	
	VGA Palette Snoop	Enables or disables VGA palette register snooping [Enabled, **Disabled]**	
	PERR# Generation	Enables or disables PCI device to generate PERR# [Enabled, **Disabled**]	
	SERR# Generation	Enables or disables PCI device to generate SERR# [Enabled, **Disabled**]	
	Above 4G Decoding	Enables or disables decoding in Address Space above '4G' for 64 bit capable devices. Note: Only if system supports 64 bit PCI decoding. [**Enabled**, Disabled]	
	SR-IOV Support	Enables or disables single root IO virtualization support If the system has SR-IOV capable PCIe devices. [**Enabled**, Disabled]	
	BME DMA Mitigation	[Enabled, **Disabled**]	
	PCI Express Settings	Relaxed ordering	Enables or disables PCI express device relaxed ordering [Enabled, **Disabled**]
		Extended Tag	If enabled the device is allowed to use 8-bit tag field as a requester. [Enabled, **Disabled**]
		No Snoop	Enables or disables PCI express device No Snoop option. [**Enabled**, Disabled]
		Maximum Payload	Sets maximum payload of PCI Express device or allows System BIOS to select the value automatically.

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description	
			[**Auto**, 128 Bytes, 256 Bytes, 512 bytes, 1024 bytes, 2048 Bytes, 4096 Bytes]
		Maximum Read Request	[**Auto**, 128 Bytes, 256 Bytes, 512 bytes, 1024 bytes, 2048 Bytes, 4096 Bytes]
		ASPM Support	[Enabled, **Disabled**]
		Warning Enabling ASPM may cause some PCI-E devices to fail.	
		Extended Synch	Allows Extended synchronization patterns. [Enabled, **Disabled**]
		Link Training Retry	Defines te number of retry attempts taken by Software to retain the link if a previous training attempt was unsuccessful [Disables, 2, 3, **5**]
		Link Training Timeout	Defines number of mssec the software waits before polling link training bit in Link status register. Range is from (10 µsec. to 10000 µsec). [**1000**]
		Unpopulated Links	Setting disable link disables unpopulated PCI express links to save power [**Keep Link On**, Disable Link]
	PCI Express GEN 2 Settings	Completion Timeout	Allows System software to modify the completion timeout value. Default range 50 µs to 50 ms. Available for device function that support Completion timeout programmability. [**Default**, Shorter, Longer, Disabled]
		ARI Forwarding	If supported by hardware and set to 'Enabled', the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type1 Configuration Request into a Type0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. Default value: Disabled [Enabled, **Disabled**]
		Atomic Op Requester Enable	If enabled and the function is supported by the hardware, AtomicOp requests are initiated only if bus master enable bit is set in the command register. [Enabled, **Disabled**]
		AtomicOP Egress Block	If enabled and the function is supported by the hardware, outbound AtomicOp requests via Egress ports are blocked. [Enabled, **Disabled**]
		IDO request Enable	If enabled and the function is supported by the hardware, the number of ID-based ordering (IDO) bit (attribute [2]) requests to be initiation is allowed to be set.

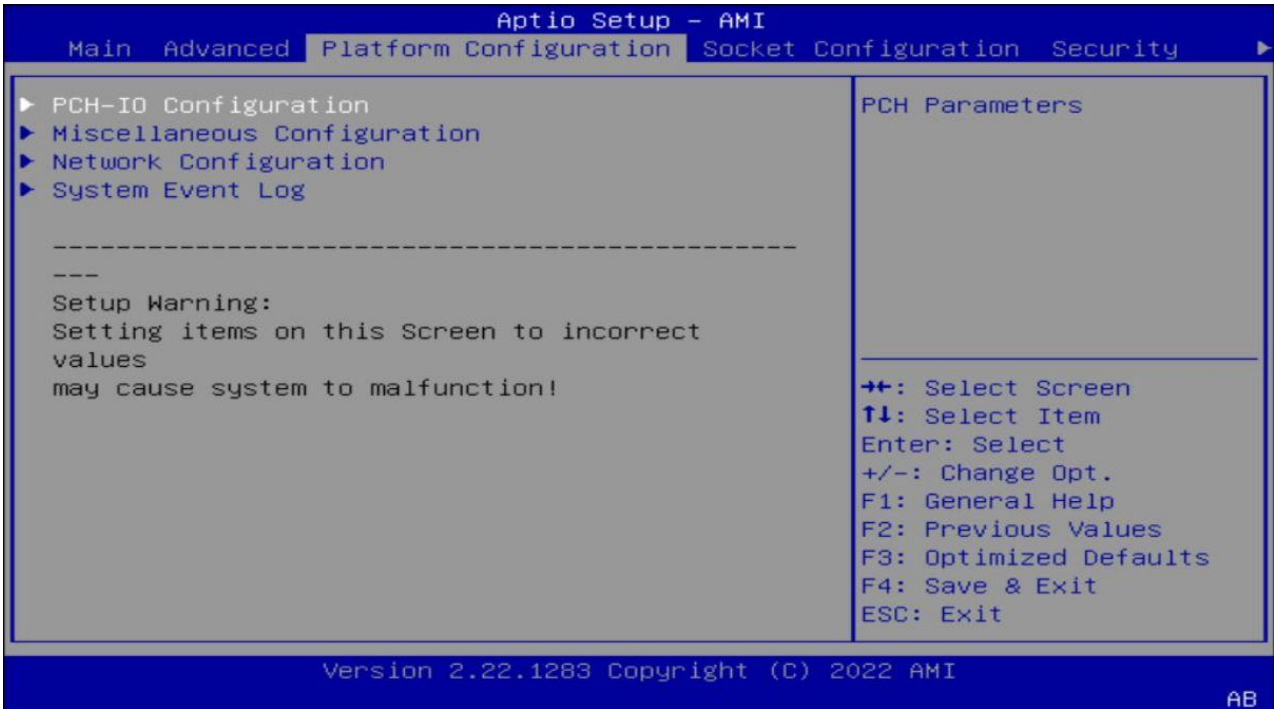
Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description	
			[Enabled, **Disabled**]
		IDO Completion Enable	If enabled and the function is supported by the hardware, the number of ID-based ordering (IDO) bit (attribute [2]) requests to be initiation is allowed to be set. [Enabled, **Disabled**]
		LTR mechanism Enable	If enabled and the function is supported by the hardware, the latency tolerance reporting (LTR) mechanism is enabled. [Enabled, **Disabled**]
		End-End TLP prefix Blocking	If enabled and the function is supported by the hardware, the forwarding of TLP containing End-End TLP prefixes is blocked. [Enabled, **Disabled**]
		Target Link Speed	If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used. [**Auto**, Force to 2.5 GT/s, Force to 5.0 GT/s]
		Clock Power management	If enabled and the function is supported by the hardware, the device is permitted to use the CLTREQ' signals for power management of the link clock in accordance to the protocol. [Enabled, **Disabled**]
		Compliance SOS	If enabled and the function is supported by the hardware, LTSSM is forced to send SKP ordered sets between sequences when sending compliance pattern or modified compliance. [Enabled, **Disabled**]
		Hardware Autonomous Width	If disabled and the function is supported by the hardware, the ability to change link width (except width size reduction for correction purposes) is disabled. [**Enabled**, Disabled]
		Hardware Autonomous Speed	If disabled and the function is supported by the hardware, the ability to change link speed (except speed rate reduction for correction purposes) is disabled. [**Enabled**, Disabled]
USB Configuration	Read only fields USB Configuration, UBS Module Version, USB Controllers, and USB devices		
	Legacy USB Support	Enables legacy USB support. Enable- Supports legacy USB Auto– disables legacy support, if no USB devices are connected Disable-keeps USB devices available only for EFI applications	

Sub-Screen	Second Level Sub-screen	Further Sub-Screens/Description
		[**Enabled**, Disabled, Auto]
	XHCI Hand-off	XHCI ownership change should be claimed by XHCI driver. Note: this is a work around for OS(s) without XHCI hand-off support. [**Enabled**, Disabled]
	USB Mass Storage Driver Support	Enables or disables USB mass storage driver support [**Enabled**, Disabled]
	USB Transfer Time-out	Displays timeout value for control, bulk and interrupt transfers [1 sec, 5 sec, 10 sec, **20 sec**]
	Device Reset Time-out	Displays USB mass storage device start unit command time-out [10 sec, **20 sec**, 30 sec, 40 sec]
	Device Power-up Delay	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor. [**Auto**, Manual]
	Mass Storage Devices	[**Auto**, Floppy, Forced FDD, Hard Disk, CD-ROM]
Network Stack Configuration	Network Stack	Enables or disables the UEFI network stack. [Enabled, **Disabled**]
NVMe Configuration	[**NVME Device**]	
SDIO Configuration	SDIO Access Mode	[**Auto**, ADMA, SDMA, PIO]
Tls Auth Configuration	Server CA Configuration	Enroll Cert, Delete Cert
	Client CA Configuration	Enroll Cert, Delete Cert
All CPU Information	Read only fields	
Emulation Configuration	uBIOS Generation	[Enabled, Disabled, **Auto**]
	Hybrid SLE Mode	[Enabled, Disabled, **Auto**]
	MSR Trace for PM	[Enabled, Disabled, **Auto**]
RAM Disk Configuration	Create raw	
	Create from file	
	Remove selected RAM disk(s)	

11.5. Platform Configuration

The Platform Configuration menu provides sub-screens and second level sub-screens for processor related functions.

Figure 15: Platform ConfigurationMenu



```
                          Aptio Setup - AMI
  Main  Advanced  Platform Configuration  Socket Configuration  Security  ►

► PCH-IO Configuration                                 PCH Parameters
► Miscellaneous Configuration
► Network Configuration
► System Event Log

  -----------------------------------------------
  ---
  Setup Warning:
  Setting items on this Screen to incorrect
  values
  may cause system to malfunction!                    →←: Select Screen
                                                      ↑↓: Select Item
                                                      Enter: Select
                                                      +/-: Change Opt.
                                                      F1: General Help
                                                      F2: Previous Values
                                                      F3: Optimized Defaults
                                                      F4: Save & Exit
                                                      ESC: Exit

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                                                                      AB
```

The following table provides an over view of the menu sub-screens and functions listed below and describes the content. Default settings are in **bold**. Some function contain additional information.

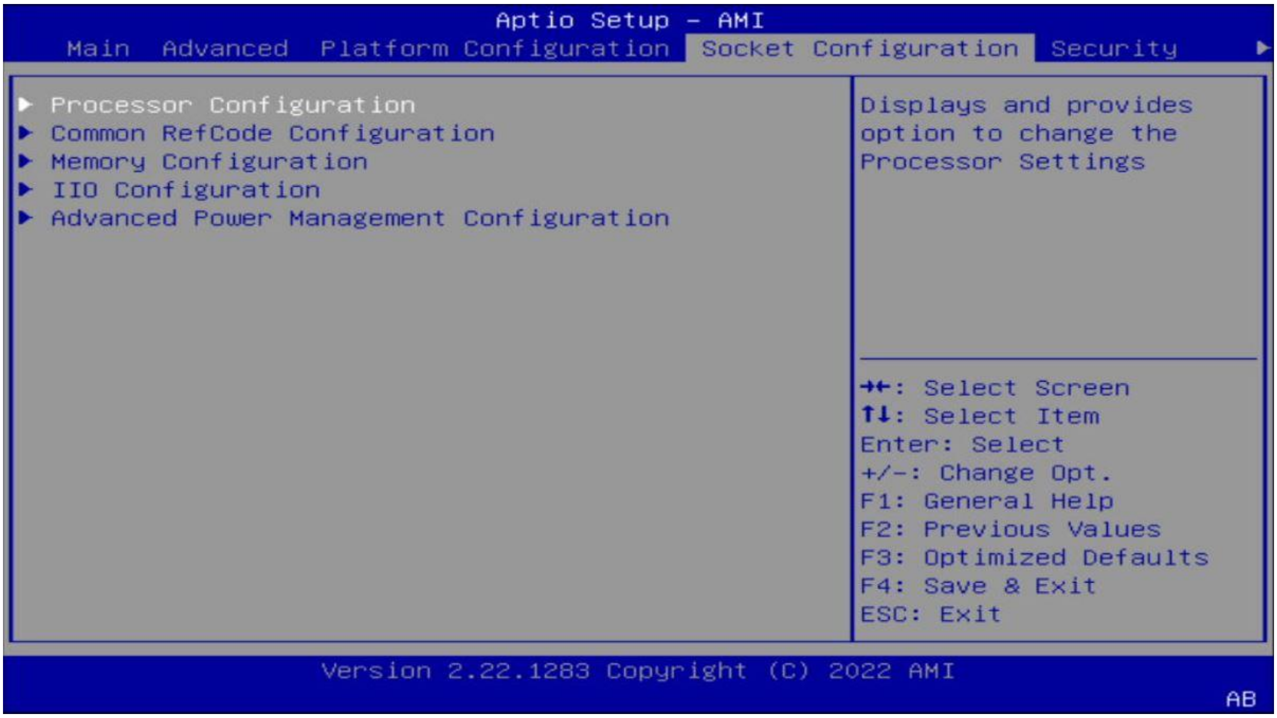
Table 35: Platform Configuration Sub-screens and Functions

Function	Description
PCH-IO Configuration	PCH Parameters
Miscellaneous Configuration	
Network Configuration	
System Event Log	Press <Enter> to view or change the event log configuration.

11.6. Socket Configuration

The Socket Configuration menu provides sub-screens and second level sub-screens for processor related functions.

Figure 16: Socket ConfigurationMenu



```
                         Aptio Setup – AMI
   Main  Advanced  Platform Configuration  Socket Configuration  Security  ►

► Processor Configuration                          Displays and provides
► Common RefCode Configuration                     option to change the
► Memory Configuration                             Processor Settings
► IIO Configuration
► Advanced Power Management Configuration

                                                   →←: Select Screen
                                                   ↑↓: Select Item
                                                   Enter: Select
                                                   +/-: Change Opt.
                                                   F1: General Help
                                                   F2: Previous Values
                                                   F3: Optimized Defaults
                                                   F4: Save & Exit
                                                   ESC: Exit

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                                                                      AB
```

The following table provides an over view of the menu sub-screens and functions listed below and describes the content. Default settings are in **bold**. Some function contain additional information.

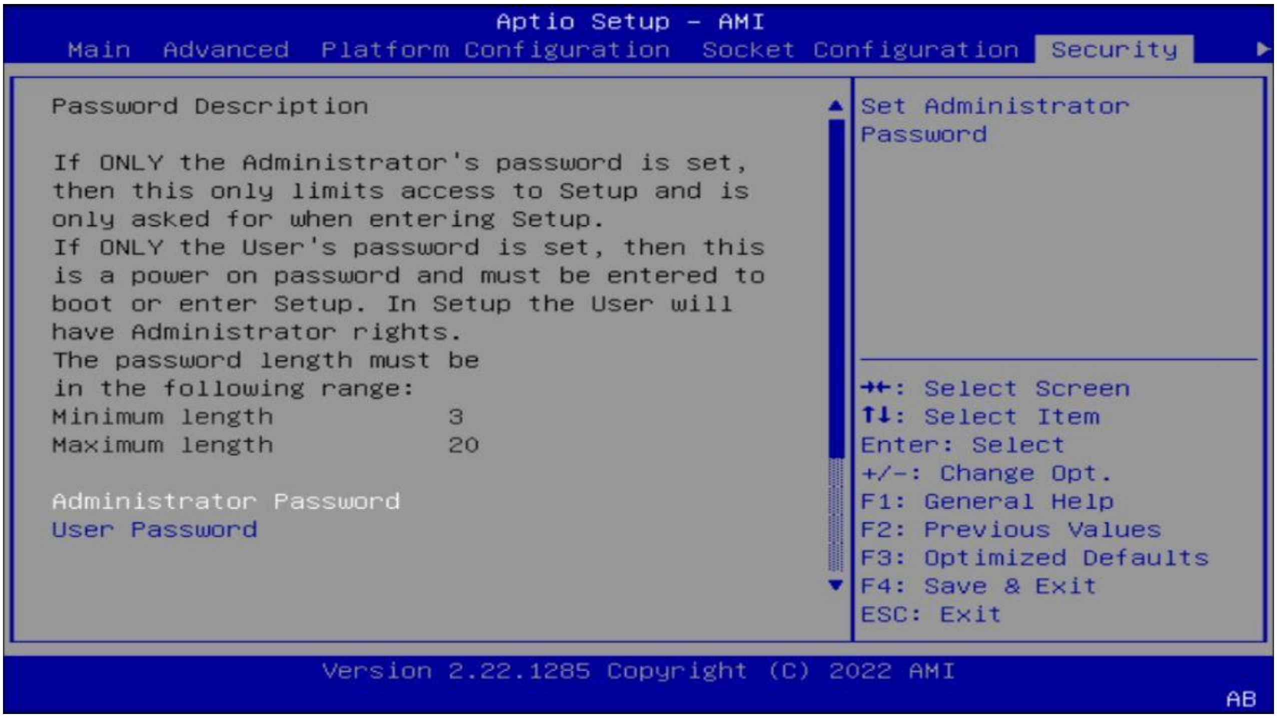
Table 36: Socket Configuration Sub-screens and Functions

Function	Description
Processor Configuration	Displays and provides option to change the Processor Settings
Common RefCode Configuration	Displays and provides option to change the Common RefCode Settings
Memory Configuration	Displays and provides option to change the Memory Settings
IIO Configuration	Displays and provides option to change the IIO Settings
Advanced Power Management Configuration	Displays and provides option to change the Power Management Settings

11.7. Security Setup Menu

The Security Setup menu provides information about the passwords and functions for specifying the security settings.

Figure 17: Security Setup Menu



```
Password Description                          Set Administrator
                                              Password
If ONLY the Administrator's password is set,
then this only limits access to Setup and is
only asked for when entering Setup.
If ONLY the User's password is set, then this
is a power on password and must be entered to
boot or enter Setup. In Setup the User will
have Administrator rights.
The password length must be                   →←: Select Screen
in the following range:                       ↑↓: Select Item
Minimum length              3                 Enter: Select
Maximum length              20                +/-: Change Opt.
                                              F1: General Help
Administrator Password                        F2: Previous Values
User Password                                 F3: Optimized Defaults
                                              F4: Save & Exit
                                              ESC: Exit
```

The following table shows Security sub-screens and functions. Default settings are in **bold**

Table 37: Security Setup Menu Functions

Function	Description		
Administrator Password	Set administrator password		
User Password	Set user password		
Secure Boot			
	Secure Boot	[Enabled, **Disabled**]	
	Secure Boot Mode	Selects the secure boot mode. Customer mode enables users to change image execution policy and manage the secure boot keys. [Standard, **Custom**]	
	Restore Factory Keys		
	Key Management	Provisional Factory Default Keys	Install factory default secure boot keys after the platform reset and while the system is in setup mode [Enabled, **Disabled**]
		Restore Factory Keys	

Function	Description		
		Platform Key	Enroll Factory Defaults or load the keys from a file with: 1. Public Key Certificate in: a. EFI_SIGNATURE_LIST b. EFI_CERT_X509 (DER encoded) c. EFI_CERT_RSA2048 (bin) d. EFI_CERT_SHA256 (bin) 2. Authenticated UEFI Variable Key source: Default, Custom, Mixed (*) modified from Setup menu
		Key Exchange Keys	
		Authorized Signatures	
		Forbidden Signatures External	
		Authorized Timestamps	
		OSRecovery Signatures	
		Export Secure Boot variables	
		Enroll Efi Image	

If only the administrator's password is set, access to the setup is limited and is requested when entering the setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. In the setup the user has administrator rights.

The required password length in characters is max. 20 and min. 3 and the passwords are case-sensitive.

11.7.1. Remember the Password

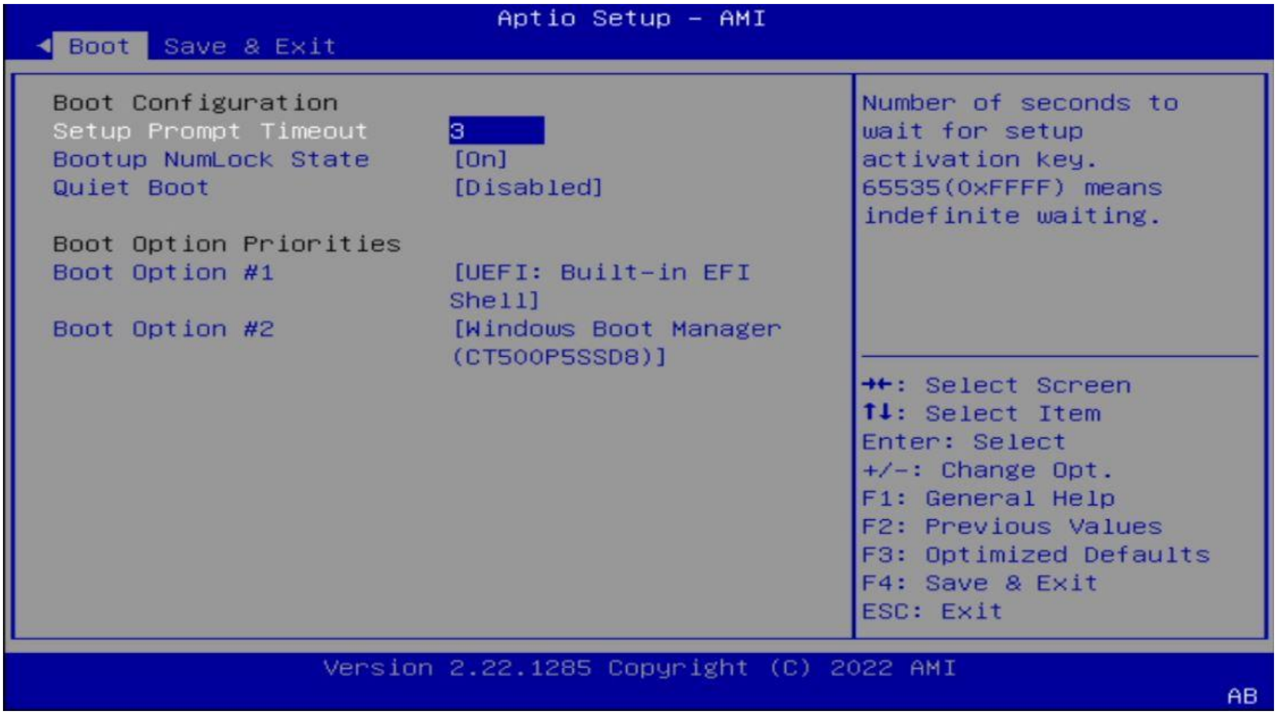
It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in the user being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not known, clear the UEFI BIOS settings, or contact Kontron Support for further assistance.

11.8. Boot Setup Menu

The Boot Setup menu lists the dynamically generated boot device priority order and the boot options.

Figure 18: Boot Setup Menu



```
                              Aptio Setup - AMI
 ◀ Boot   Save & Exit

   Boot Configuration                              Number of seconds to
   Setup Prompt Timeout       3                    wait for setup
   Bootup NumLock State       [On]                 activation key.
   Quiet Boot                 [Disabled]           65535(0xFFFF) means
                                                   indefinite waiting.
   Boot Option Priorities
   Boot Option #1             [UEFI: Built-in EFI
                              Shell]
   Boot Option #2             [Windows Boot Manager
                              (CT500P5SSD8)]
                                                   →←: Select Screen
                                                   ↑↓: Select Item
                                                   Enter: Select
                                                   +/-: Change Opt.
                                                   F1: General Help
                                                   F2: Previous Values
                                                   F3: Optimized Defaults
                                                   F4: Save & Exit
                                                   ESC: Exit

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                                                                    AB
```

The following table shows Boot sub-screens and functions, and describes the content. Default settings are in **bold**.

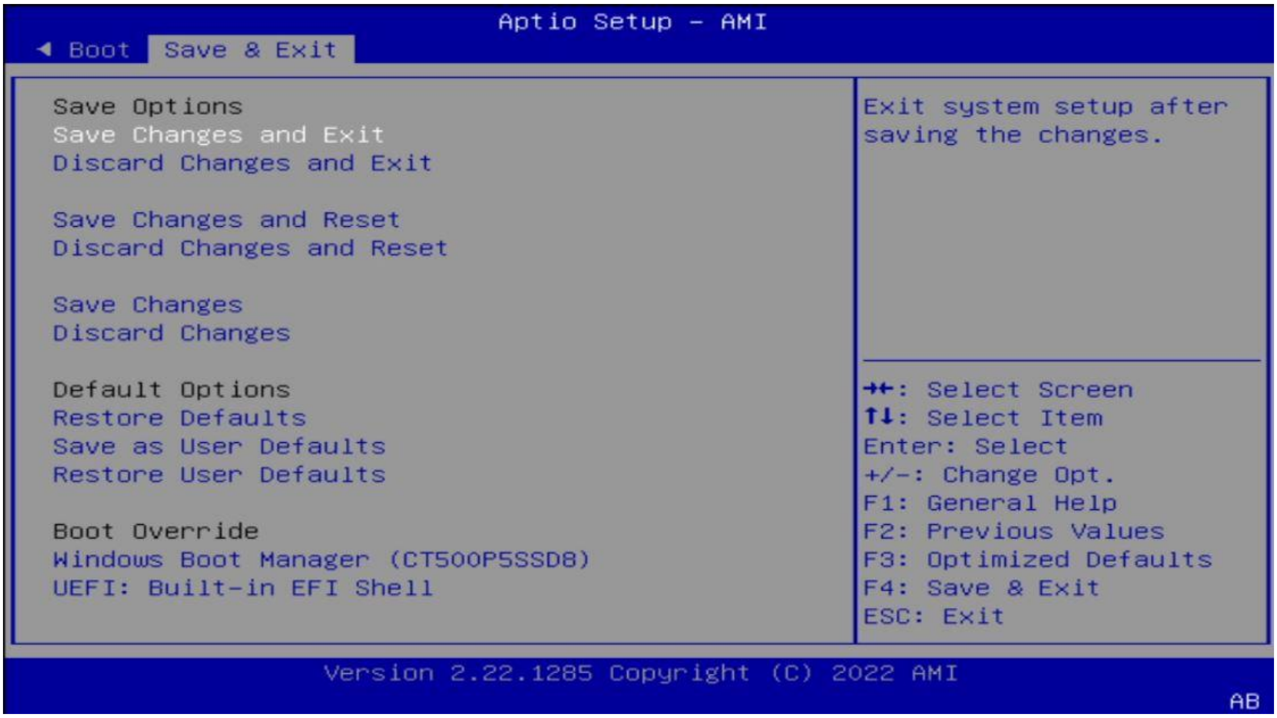
Table 38: Boot Setup Menu Functions

Function	Description
Setup Prompt Timeout	Displays number of seconds to wait for the setup activation key. 65535(OXFFF) means indefinite waiting [**3**]
Bootup NumLock State	Selects keyboard NumLock state [**On**, Off]
Quiet Boot	Enables or disables Quiet Boot [Enabled, **Disabled**]
Boot Option #1	Sets the system boot order (option 1) [**UEFI Built-in EFI shell**, Disabled]
Boot Option #2	Sets the system boot order (option 2) [UEFI Built-in EFI shell, **Windows Boot Manager**, Disabled]

11.9. Save and Exit

The Save and Exit Setup menu lists the save, default and override options.

Figure 19: Save and Exit Setup Menu



```
                         Aptio Setup - AMI
 ◄ Boot  Save & Exit

  Save Options                                Exit system setup after
  Save Changes and Exit                       saving the changes.
  Discard Changes and Exit

  Save Changes and Reset
  Discard Changes and Reset

  Save Changes
  Discard Changes

  Default Options                             →←: Select Screen
  Restore Defaults                            ↑↓: Select Item
  Save as User Defaults                       Enter: Select
  Restore User Defaults                       +/-: Change Opt.
                                              F1: General Help
  Boot Override                               F2: Previous Values
  Windows Boot Manager (CT500P5SSD8)          F3: Optimized Defaults
  UEFI: Built-in EFI Shell                    F4: Save & Exit
                                              ESC: Exit

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                                                                  AB
```

The following table shows Boot sub-screens and functions, and describes the content. Default settings are in bold.

Table 39: Save and Exit Menu Functions

Function	Description
Save Options	
Save Changes and Exit	Exits system after saving changes
Discard Changes and Exit	Exits system setup without saving changes
Save Changes and Reset	Resets system after saving changes
Discard Changes and Reset	Resets system setup without saving changes
Save Changes	Saves changes made so far for any setup options
Discard Changes	Discards changes made so far for any setup options
Default Options	
Restore Defaults	Restores/loads standard default values for all setup options
Save as User Defaults	Saves changes made so far as User Defaults
Restore User Defaults	Restores User Defaults to all setup options
Boot Override Options	
Windows Boot Manager	Attempts to launch the Windows Boot Manager
UEFI Built-in EFI shell	Attempts to launch the built in EFI Shell

11.10. The UEFI Shell

The Kontron UEFI BIOS features a built-in and enhanced version of the UEFI Shell. For a detailed description of the available standard shell scripting, refer to the EFI Shell User Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage (http://sourceforge.net/projects/efi-shell/files/documents/).

AMI APTIO update utilities for DOS, EFI Shell and Windows are available at AMI.com: http://www.ami.com/support/downloads/amiflash.zip.

Kontron UEFI BIOS does not provide all shell commands described in the EFI Shell Command Manual.

11.10.1. Basic Operation of the UEFI Shell

The UEFI Shell forms an entry into the UEFI boot order and is the first boot option by default.

11.10.1.1. Entering the UEFI Shell

To enter the UEFI Shell, follow the steps below:

1. Power on the board.
2. Press the <F7 key (instead of <DEL) to display a choice of boot devices.
3. Choose ‘UEFI: Built-in EFI shell’.

```
EFI Shell version 2.40 [5.11]
Current running mode 1.1.2
Device mapping table
Fs0      :HardDisk - Alias hd33b0b0b fs0
   Acpi(PNP0A03,0)/Pci(1D|7)/Usb(1, 0)/Usb(1, 0)/HD(Part1,Sig17731773)
```

4. Press the <ESC key within 5 seconds to skip startup.nsh, and any other key to continue.

The output produced by the device mapping table can vary depending on the board's configuration.

If the <ESC key is pressed before the 5 second timeout elapses, the shell prompt is shown:

```
Shell
```

11.10.1.2. Exiting the UEFI Shell

To exit the UEFI Shell, follow one of the steps below:

1. Use the exit UEFI Shell command to select the boot device, in the Boot menu, that the OS boots from.
2. Reset the board using the reset UEFI Shell command.

11.11. UEFI Shell Scripting

11.11.1. Startup Scripting

If the <ESC key is not pressed and the timeout has run out then the UEFI Shell automatically tries to execute some startup scripts. It searches for scripts and executes them in the following order:

1. Initially searches for Kontron flash-stored startup script.
2. If there is no Kontron flash-stored startup script present, then the UEFI-specified startup.nsh script is used. This script must be located on the root of any of the attached FAT formatted disk drive.
3. If none of the startup scripts are present or the startup script terminates then the default boot order is continued.

11.11.2. Create a Startup Script

Startup scripts can be created using the UEFI Shell built-in editor edit or under any OS with a plain text editor of your choice. To create a startup shell script, simply save the script on the root of any FAT-formatted drive attached to the system. To copy the startup script to the flash, use the kBootScript UEFI Shell command.

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the kRamdisk UEFI Shell command.

11.12. Example of Startup Scripts

11.12.1. Execute Shell Script on other Harddrive

This example (startup.nsh) executes the shell script named bootme.nsh located in the root of the first detected disc drive (fs0).

```
        fs0:
        bootme.nsh
```

11.13. Firmware Update

Firmware updates are typically delivered as a ZIP archive. Please find the latest available BIOS-ZIP archive on Kontron's Customer Section. Further information about the firmware update procedure can be found in the included "flash_instruction.txt"-file.

i Register for Kontron's Customer Section to get access to BIOS downloads and PCN service.

12/ Technical Support

For technical support contact our Support department:

E-mail:	support@kontron.com
Phone:	+49-821-4086-888

Make sure you have the following information available when you call:

Product ID Number (PN),
Serial Number (SN)
Module's revision
Operating System and Kernel/Build version
Software modifications
Addition connected hardware/full description of hardware set up

The serial number can be found on the Type Label, located on the product's rear side.

Be ready to explain the nature of your problem to the service technician.

12.1. Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law. This applies to the CMOS battery, for example.

If there is a protection label on your product, then the warranty is lost if the product is opened.

12.2. Returning Defective Merchandise

All equipment returned to Kontron must have a Return of Material Authorization (RMA) number assigned exclusively by Kontron. Kontron cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to Kontron's designated facility. Kontron will pay the return freight charges back to the buyer's location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to Kontron.

1. Visit the RMA Information website:
https://www.kontron.com/en/support/rma-information

Download the RMA Request sheet for Kontron Europe GmbH and fill out the form. Take care to include a short detailed description of the observed problem or failure and to include the product identification Information (Name of product, Product number and Serial number). If a delivery includes more than one product, fill out the above information in the RMA Request form for each product.

2. Send the completed RMA-Request form to the fax or email address given below at Kontron Europe GmbH. Kontron will provide an RMA-Number.

   Kontron Europe GmbH
   RMA Support
   Phone: +49 (0) 821 4086-0
   Fax: +49 (0) 821 4086 111
   Email: service@kontron.com

3. The goods for repair must be packed properly for shipping, considering shock and ESD protection.

Goods returned to Kontron Europe GmbH in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

Include the RMA-Number with the shipping paperwork and send the product to the delivery address provided in the RMA form or received from Kontron RMA Support.

Appendix: Terminology

Term	Definition
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PCAT systems
Basic Module	COM Express® 125mm x 95mm Module form factor.
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system.
Carrier Board	An application specific circuit board that accepts a COM Express® Module.
Compact Module	COM Express® 95x95 Module form factor
DDI	Digital Display Interface – containing DisplayPort, HDMI/DVI and SDVO
DIMM	Dual In-line Memory Module
DRAM	Dynamic Random Access Memory
EAPI	Embedded Application Programming Interface Software interface for COM Express® specific industrial functions System information Watchdog timer I2C Bus Flat Panel brightness control User storage area GPIO
EEPROM	Electrically Erasable Programmable Read-Only Memory
Extended Module	COM Express® 155mm x 110mm Module form factor.
Gb	Gigabit
GbE	Gigabit Ethernet
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
I2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values.
IIO	Integrated Input Output
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
ME	Management Engine
Mini Module	COM Express® 84x55mm Module form factor

Term	Definition
NA	Not Available
NC	No Connect
PCB	Printed Circuit Board
PCI Express PCIE	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PEG	PCI Express Graphics
PHY	Ethernet controller physical layer device
Pin-out Type	A reference to one of seven COM Express® definitions for the signals that appear on the COM Express® Module connector pins.
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
RP	Root Port
RPC	Root Complex
SAS	Serial Attached SCSI – high speed serial version of SCSI
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information
SPI	Serial Peripheral Interface
SO-DIMM	Small Outline Dual In-line Memory Module
S0, S1, S2, S3, S4, S5	System states describing the power and activity level S0 Full power, all devices powered S1 S2 S3 Suspend to RAM System context stored in RAM; RAM is in standby S4 Suspend to Disk System context stored on disk S5 Soft Off Main power rail off, only standby power rail present
SATA	Serial AT Attachment: serial-interface standard for hard disks
TPM	Trusted Platform Module, chip to enhance the security features of a computer system.
USB	Universal Serial Bus
WDT	Watch Dog Timer
x1	Refers to a Link or Port with one Physical Lane.
x4	Refers to a Link or Port with four Physical Lanes.
x8	Refers to a Link or Port with eight Physical Lanes.
x16	Refers to a Link or Port with sixteen Physical Lanes.

About Kontron

Kontron is a global leader in IoT/Embedded Computing Technology (ECT). Kontron offers individual solutions in the areas of Internet of Things (IoT) and Industry 4.0 through a combined portfolio of hardware, software and services. With its standard and customized products based on highly reliable state-of-the-art technologies, Kontron provides secure and innovative applications for a wide variety of industries. As a result, customers benefit from accelerated time-to-market, lower total cost of ownership, extended product lifecycles and the best fully integrated applications.

For more information, please visit: **www.kontron.com**

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